SIGE BICMOS PHASED-ARRAY ANTENNA FRONT-ENDS FOR EXTREME ENVIRONMENT APPLICATIONS

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SUMMARY

The objective of this research is to understand the design and performance of state-of-the-art silicon-germanium (SiGe) BiCMOS high-frequency circuits for phased-array radar and wireless communication systems operating in extreme environment conditions. This work investigates the performance of RF circuits over a wide-temperature and exposure to a radiation intensive environment. The design and characterization of a fully integrated transmit/receive (T/R) module and integration onto a multi-element antenna array is presented. In addition, individual circuit blocks are characterized in these extreme environments. The following is a summary contributions:

1. Design and characterization of SiGe HBT based X-band LNAs [74, 78, 81].

2. Development of an integrated SiGe BiCMOS X-band T/R module and assembly of 64 element active phased-array receive antenna [72].

3. Design of on-wafer wide-temperature noise figure measurement setup and characterization of low-temperature noise figure of SiGe HBT devices and LNAs [82].

4. Design of on-wafer wide-temperature two-tone linearity measurement setup using a network analyzer and signal generator and measurement of a low-power LNA from 173 to 300 K.

5. Investigation of total dose radiation effects on BiCMOS phase shifters [77].

6. Design of a novel SiGe HBT based device, called the inverse-mode cascode (IMC), for use in radiation tolerant digital circuits [75].

CHAPTER I

INTRODUCTION

1.1 Motivation

Silicon-Germanium (SiGe) hetrojunction bipolar transistor (HBT) technology has made great in-roads for high-performance, radio-frequency (RF) and millimeter wave (mmW) communication and radar applications. Over the past decade, the performance of SiGe HBTs has greatly increased, rivaling more costlier, III-V based technologies [65]. These advances have made it possible to design demanding phased-array antenna components and systems using this lower cost technology and still satisfy strict performance specifications.

In addition to terrestrial based systems, the use of these inexpensive technologies in space-based orbital or extra-terrestrial applications would provide many benefits including lower cost and higher integration levels, yielding compact and inexpensive space electronics [16]. These "extreme environment" applications places additional requirements on the technology including: radiation tolerance and wide-temperature operation. In order to implement these high-frequency phased-array systems for extreme environment applications, a thorough investigation of both radiation effects and wide-temperature operation on the performance of SiGe BiCMOS circuits is required and has not been conducted to date. The research presented in this thesis aims to provide insight into the design and measurement of the components that are part of the front-end modules for these phased-array antenna systems.

1.1.1 Silicon-Germanium Hetrojunction Bipolar Transistor Technology

SiGe HBTs combines the speed and performance of many III-V technologies with Si-processing compatibility yielding a high-performance device that is readily commercially available. Since the first SiGe HBT demonstration over 20 years ago, SiGe HBT technology has shown an almost exponential growth both in terms of performance and number of commercial facilities as shown in Figure 1 and 2 [20, 21].

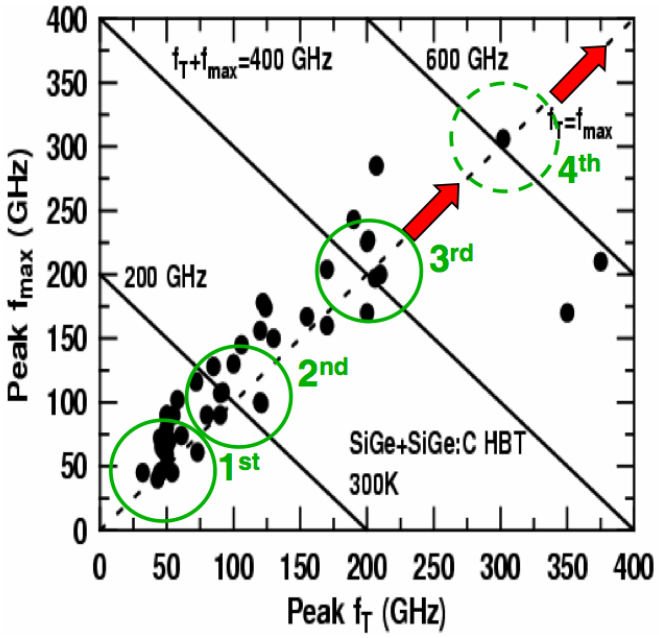


Figure 1: SiGe HBT technology performance growth as measured by f_t and f_{max} [20].

SiGe technology uses band-gap engineering in the base of a Silicon Bipolar Junction Transistor (BJT) to enhance device characteristics. By epitaxially growing compositionally graded SiGe alloy as the transistor base, device parameters are decoupled allowing exponential "tuning" based on the Ge content. The mechanism for this tuning capability is driven by the bandgap difference between Si (1.12 eV at 300 K) and Ge (0.66 eV at 300 K). This difference allows the bandgap of the SiGe alloy to be optimized to improve transistor performance. The effect of the graded Ge in the base directly impacts key performance metrics such as current gain (β), base transit time (τ_b), cutoff frequency (f_T) and maximum oscillation frequency (f_{max}), which couple

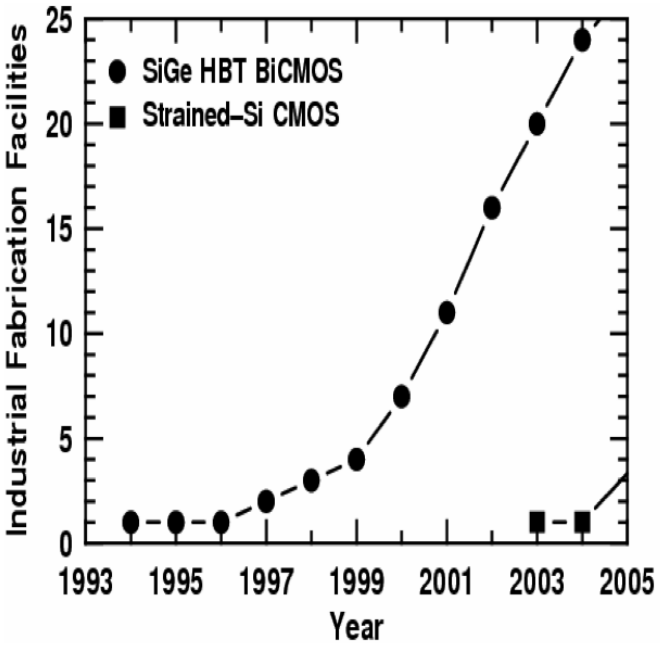


Figure 2: SiGe HBT technology commercial fabrication facilities [20].

strongly to high-frequency amplifier performance.

A comparison of these parameters between a standard Si BJT and SiGe HBT yields an understanding of how Ge content can influence device performance. Assuming a linearly graded Ge profile (Figure 3), the collector current density enhancement directly relates to the β enhancement between a SiGe HBT and a Si BJT [20]:

$$\frac{J_{C,SiGe}}{J_{C,Si}} \simeq \frac{\beta_{SiGe}}{\beta_{Si}} \simeq \frac{\tilde{\gamma}\tilde{\eta}\Delta E_{g,Ge}(grade)/kTe^{\Delta E_{g,Ge}(0)/kT}}{1-e^{-\Delta E_{g,Ge}(grade)/kT}} \tag{1}$$

where $\tilde{}$ denotes the positioned averaged quantities across the base, γ is the "effective density-of-states" ratio and η is the minority electron diffusivity ratio between SiGe and Si. The Ge profile enters the relationship through $\Delta E_{g,Ge}(grade)$ which is defined as $E_{g,Ge}(Wb) - E_{g,Ge}(0)$. This equation shows that as $\Delta E_{g,Ge}(grade)$ is increased, the total current gain will also increase. In addition, this enhancement is temperature activated through the $1/kT$ term. This relative enhancement in β has an impact on high frequency amplifier performance in terms of gain and noise figure.

Further analysis shows that two crucial metrics of device performance, f_T and

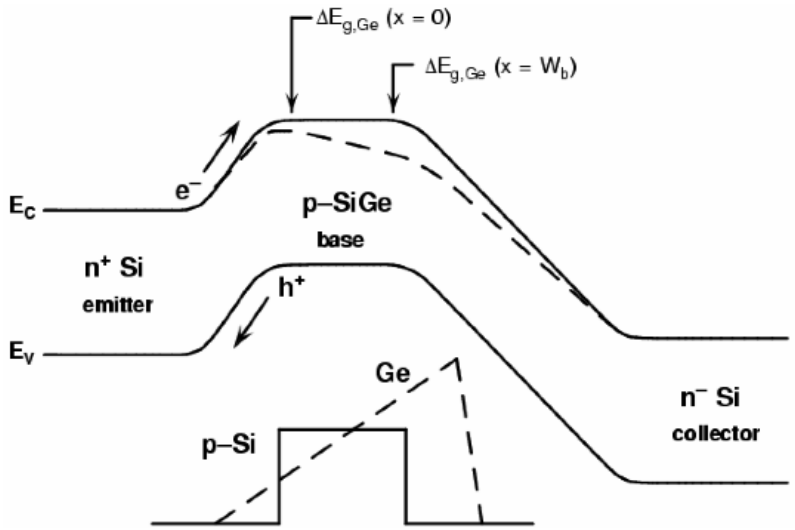


Figure 3: Energy band diagram for SiGe HBT (dashed) compared to Si BJT (solid) biased in the forward active region [20]

f_{max}, are largely enhanced through the minimization of τ_b through the addition of Ge in the base. Assuming a strong Ge grading scenario, which is true for the current generation of HBT technologies, τ_b is improved by $\Delta E_{g,Ge}(grade)$:

$$\tau_{b,SiGe} \simeq \frac{W_b^2}{2\tilde{D_{nb}}} \frac{kT}{\Delta E_{g,Ge}(grade)} \tag{2}$$

where W_b is the base width and D_{nb} is the minority electron diffusivity. By increasing $\Delta E_{g,Ge}(grade)$, τ_b is reduced. Also, τ_e (emitter charge storage delay) is proportional to $1/\beta$ therefore resulting in a reduction of the total transit time. This can be further explored by examining f_T:

$$f_T = \frac{1}{2\pi} \left[\frac{1}{g_m}(C_{te} + C_{tc}) + \tau_b + \tau_e + \frac{W_{CB}}{2v_{sat}} + r_c C_{tc} \right]^{-1} \tag{3}$$

where g_m is the device transconductance ($\delta I_c / \delta V_{BE}$), $C_{te} + C_{tc}$ are the depletion capacitances, W_{CB} is the junction width of the collector-base (CB) space charge region, v_{sat} is saturation velocity, and r_c is the small-signal collector resistance. Since f_T is inversely proportional to τ_b and τ_e, their reduction will increase f_T. Also, f_{max} will improve since it is a function of f_T:

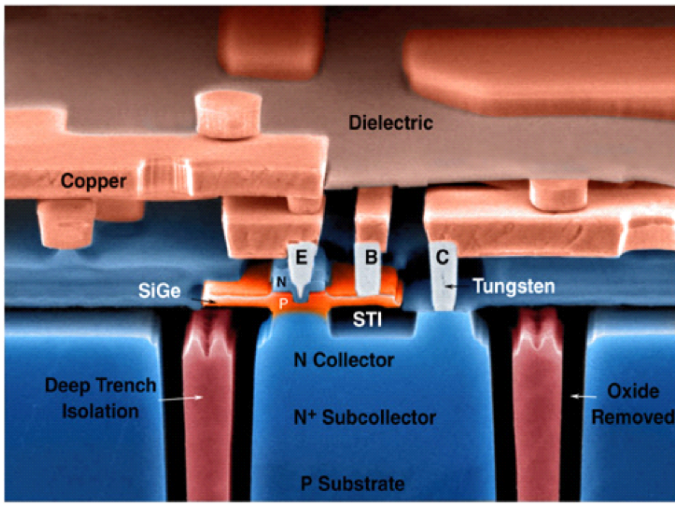


Figure 4: Structure of third-generation SiGe HBT (courtesy of IBM).

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{bc} r_b}} \tag{4}$$

where C_{bc} is the collector base capacitance, and r_b is the intrinsic base resistance. By adjusting the Ge grading, higher base doping can be used while still maintaining a high β, yielding a lower base resistance and improved noise performance. These performance parameters point to the ability to increase such amplifier characteristics such as gain and noise figure, which can greatly benefit high-frequency design.

One of the key advantages of SiGe HBT technology is its compatibility with traditional Si CMOS processing. The Ge layer is grown using a ultra-high vacuum/chemical vapor deposition (UHV/CVD) processing step, which reduces the necessary thermal cycle and has fine control of the Ge profile. This process modification is typically included as a "plug-in module" in traditional Si CMOS fabrication facilities allowing for a high-yielding low-cost BiCMOS technology [21]. A micrograph of a cross-section of a third-generation SiGe HBT is shown in Figure 4. SiGe HBTs compatibility with Si CMOS processing is a key advantage over competing III-V technologies which are typically characterized by low to moderate-yielding, non-Si CMOS

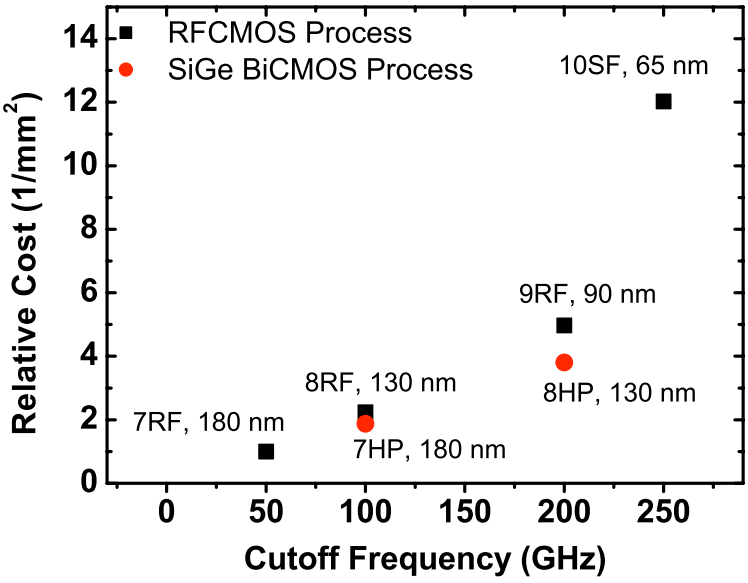


Figure 5: Comparison of normalized trusted foundry pricing as a function of f_T for Si CMOS and SiGe HBTs at various technology nodes (2008 prices, courtesy of P. Cheng.

compatible processing. In addition, the performance improvements at a given technology node allow SiGe HBTs to provide cost vs performance advantage even over Si-CMOS. Figure 5 compares RFCMOS versus SiGe HBT relative trusted foundry pricing at a similar technology performance as measured by f_T. Relevant performance specifications for a third generation SiGe technology are highlighted in Table 1.

Table 1: Typical SiGe HBT third generation device performance parameters

W_E	0.12 μm
peak β	400
peak f_T	200 GHz
peak f_{max}	250 GHz
J_c @ peak f_T	5-10 mA/μm^2
BV_{CEO}	1.8 V

1.1.2 Active Phased-Array Antennas Systems

Many new communication and radar systems rely on active phased-array antenna systems, increasingly implementing these circuits in Si-based platforms [26] . Unlike traditional horn or dish antennas, phased-array antenna systems achieve directionality by using constructive and destructive phase interference between different antenna elements to create a steerable beam. Electronically scanned arrays (ESAs) have been used for many years in non-commerical applications, and use a passive phase shifter at each antenna element to dynamically steer the beam. As microelectronics continues to increase performance and decrease in size, these systems are giving way to the next generation active electronically scanned arrays (AESAs), in which each antenna element contains active circuit blocks to perform the receive and transmit functions. A example of this technology is a National Oceanic and Atmospheric Administration (NOAA) weather radar system as shown in Fig. 6, which yields over a six times improvement in scan rate and weather tracking over the previous radar system [56].

Figure 6: National Oceanic and Atmospheric Administration (NOAA) phased-array weather radar system [56].

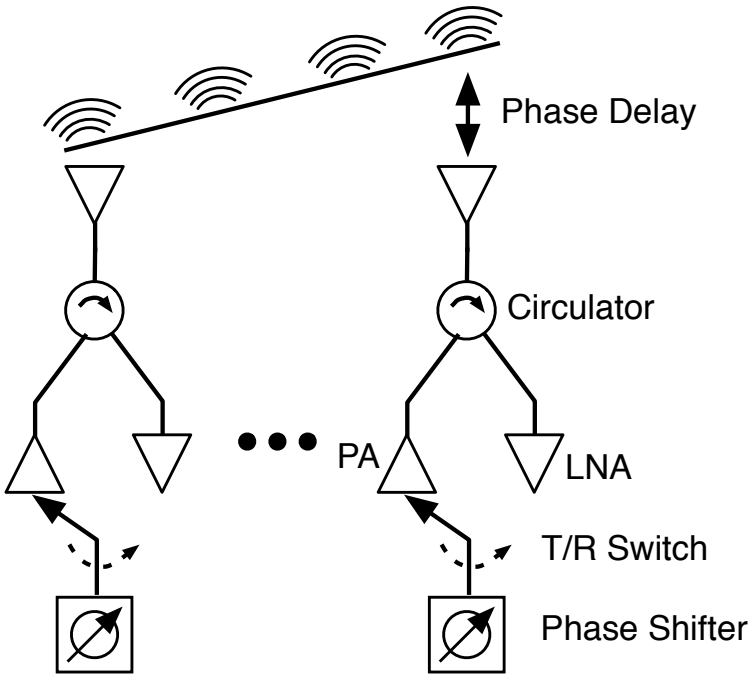


Figure 7: Typical active phased-arrary antenna topology for wireless communication and radar systems.

A key building block in active phased-array systems is the transmit/receive (T/R) antenna module. A T/R module typically consists of a low-noise amplifier (LNA), power amplifier (PA), T/R switch, circulator, and phase shifter (PS) (Fig. 7). In the past, this module used III-V circuit components (such as GaAs) in costly multi-component modules (MCMs) that cost in the thousands of dollars per unit. As highlighted in section 1.1.1 the performance improvements and low-cost of SiGe technology is allowing its use in high performance systems. By integrating all of these functions onto a single SiGe BiCMOS chip, drastic cost and size saving could be achieved, while still achieving the required performance.

The LNA is the first amplifier in the receive chain and enhances sensitivity by reducing total overall system noise figure. The key specifications for the LNA are noise figure, gain, and linearity. The PA provides high-power amplification to the antenna while providing ample gain, low-power dissipation, and low-signal distortion.

The T/R switch allows the use of a common bidirectional phase shifter and allowing switching between receive and transmit mode operation. Phase shifters change the phase of the RF signal to produce an effective time delay. Each phase shifter in a TR module should have a programmable 0-360 degrees of phase control to produce phase differences between each T/R element, enabling scanning of the antenna beam.

1.1.3 Extreme Environment Applications

Extreme environments are considered as those surroundings outside conventional commercial or military limits for electronic parts [17]. This niche market does not have the economics of scale as in commercial IC fabrication to drive low-cost production. The process modifications necessary for extreme environment applications add significant cost to these electronic systems. These applications could greatly benefit by using commercial fabrication technology that has the ability operate in harsh environments. Typical extreme environments include outside the mil-spec temperature range (-55°C to 125°C), radiation environment, high/low pressures, and chemically corrosive environment. The research presented in this thesis focuses on wide-temperature and radiation extreme environment applications.

Wide-temperature operation of electronics are challenging due to substantial changes in device performance over temperature. In addition, RF circuits are sensitive to device bias currents and parasitics, which change over temperature. Lastly, typical foundry provided design kits provide accurate models to commercial or military specifications, therefore in order to design over wide-temperature ranges, custom device models need to be designed. The first step in this process is to characterize the RF performance of devices and circuits across these wide-temperature ranges.

Radiation intensive extreme environment poses a different set of challenges over the wide-temperature operation. Radiation can affect circuits in multiple methods including total ioninzing dose (TID) effects and single-event effects (SEEs) as shown in

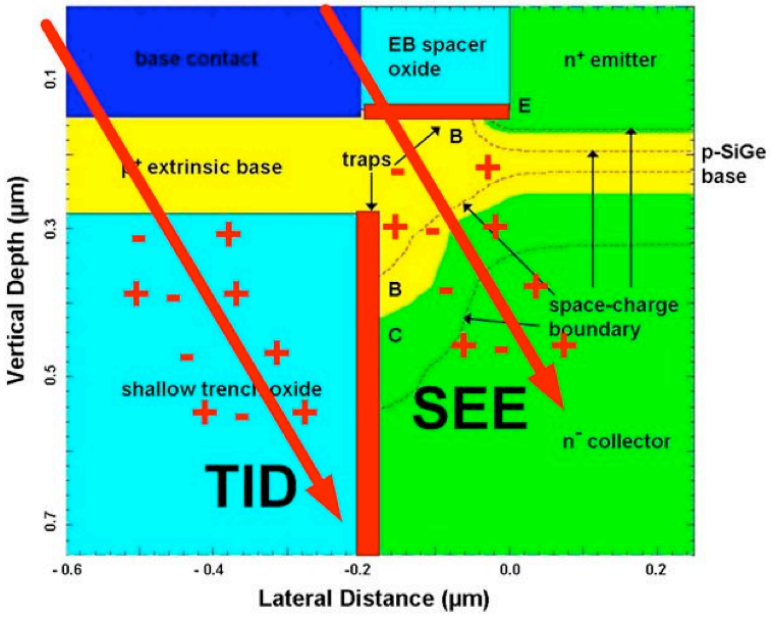


Figure 8: Profile of SiGe HBT highlighting areas affected by total ioninzing dose (TID) and single-event effects (SEEs) (courtesy of A. Sutton).

Fig 8. TID radiation effects are attributed to particles (such as gamma rays, neutrons, and protons) causing either displacement or ionization damage to the device. These effects can cause permanent damage to the device and degrade operation of the circuit. SEEs are due to single energetic particles and cause transients in the device and can cause a disruption of the signal. Both of these effects can cause disruptions to the RF signal as well as to the digital/analog control that could degrade circuit performance.

1.2 Purpose of Research

The purpose of this research is to understand the design constraints for high-frequency SiGe BiCMOS circuits used in extreme environment phased-array antenna applications. Much of the current literature highlighting extreme environment applications discusses SiGe HBTs in the context of *dc* and analog applications. However, there is significant interest in using this low-cost, high-performance technology for high-frequency extreme environment applications.

Characterization of SiGe HBTs at cryogenic temperature has shown large performance improvements in cooling [92], However, it is not clear how to best optimize RF circuits for wide-temperature operation. Many RF parameters (noise, linearity, etc) are directly tied to the bias currents in the transistors and the optimum bias conditions over wide-temperature range requires further investigation. However, accurate characterization of these higher order circuit parameters are difficult due to measurement challenges, and require the development of novel measurement techniques.

In addition, radiation effects on SiGe BiCMOS circuits has primarily focused on analog and digital applications. Much of the high-frequency work in this field has focused on TID validation to show performance degradation due to damage to the device. Radiation effects on high-frequency circuits becomes increasingly critical in highly integrated phased-array transmit/recieve (T/R) modules that could contain both RF, analog, and digital blocks. SEEs in active T/R modules could lead to serious performance degradations of the antenna system and it is not clear what impact this irradiation could have on the operation and control of these modules.

The research presented in this thesis aims to demonstrate the design and characterization of high-frequency circuits in SiGe HBT technology and conduct experimental studies to determine the impacts of wide-temperature operation and radiation effects on T/R module building blocks used in phased-array antenna front-ends. These blocks include low-noise amplifiers, phase shifters, and digital control circuitry. The purpose of these studies is to understand the circuit response to extreme environments and determine methods to best optimize these building blocks.

1.3 Objective and Contributions of this work

This thesis contributes to the understanding of designing and the optimization of RF front-ends for phased-array antenna systems. These contributions include: (1) design and characterization of LNA building blocks [74, 78, 81], (2) design and optimization of a T/R module for phased-array antennas [72, 80], (3) analysis of wide-temperature operation of RF circuit building blocks [82], and (4) analysis of phased-array antenna modules components in a radiation environment [75–77].

Recently, SiGe BiCMOS technology has gained favor for many phased-array antenna systems, with emphasis placed on using SiGe circuits for the T/R modules in phased-array radar systems [15]. Components for RF front-ends have been designed, developed, and optimization schemes have been introduced, focusing on trade-offs necessary for the given design constraints. Chapter 2 of this thesis presents the design of a ultra-low power LNA, a high-dynamic range LNA, and the characterization of LNAs under high RF power. This chapter aims to demonstrate different design optimization schemes for the development of high-frequency LNAs.

The research documented in chapter 3 presents the design of T/R modules and highly-integrated active phased-array antennas using SiGe BiCMOS technology. My role in this research was the development of the SiGe T/R module, assistance with packaging and integration of the T/R module onto the antenna array, and measurement of the antenna array.

Chapter 4 of this thesis presents research to help improve the understanding of SiGe HBT devices and circuits operating over wide-temperatures. Specifically, novel noise figure and linearity measurement techniques are presented. These techniques are verified using devices and circuits, which can be used to extend high-frequency device models and aid in the development of RF circuits for wide-temperature operation.

The final research that is presented in this thesis in chapter 5 is to further understand circuit irradiation on phased-array antenna performance, specifically focusing

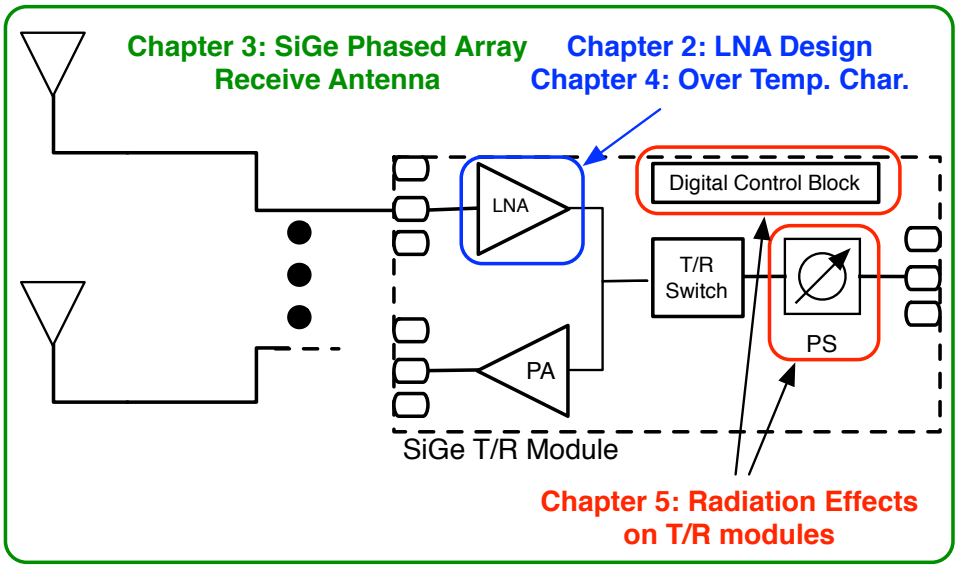


Figure 9: Block level diagram of T/R module depicting an outline of topics covered within this thesis.

on the phase-shifters and digital control blocks. Understanding the manner in which phased-array antennas systems might degrade in a radiation environment is necessary if these types of systems are to be deployed in extreme environments, such as space.

To better understand the research covered within this thesis, a visual summary of the topics presented is shown in Fig. 9. To conclude, chapter 6 summarizes the results of this work, as well as presents possible extension of this research for future follow-on work.

A significant amount of this work has been published or submitted for publication at various refereed conferences and journals, including IEEE Radio Frequency Integrated Circuits Symposium [74], IEEE Microwave and Wireless Components Letters [82],IEEE Transactions on Nuclear Science [75, 77], IEEE European Microwave Integrated Circuits Conference [79], IEEE Bipolar/BiCMOS Circuits and Technology Meeting [76, 80], IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems [78,81], and IEEE Transaction on Microwave Theory and Techniques [72]. Master level research prior to this work was completed in 2007 [73]. More specifically, details of this dissertation can be found in the following refereed publications:

1. Design and characterization of an ultra-low power SiGe HBT based X-band low-noise amplifier (Section 2.1, also published in [74]).

2. Design and characterization of high dynamic range SiGe HBT based X-band low-noise amplifier (Section 2.2, also published in [78]).

3. Characterization of large-signal robustness of SiGe HBT based X-band low-noise amplifiers (Section 2.3, also published in [81]).

4. Design of a 64-element receive SiGe active X-band phased-array antenna on a multi-layer organic substrate (Chapter 3, submitted for review in [72]).

5. Cryogenic Noise Measurement of packaged SiGe HBT LNAs (Section 4.3, also published in [82]).

6. Total Ionizing Dose Phase Shifter Irradiation (Section 5.1, also published in [77]).

7. Novel Radiation Hardening by Design Technique for Single Event Effect Mitigation (Section 5.2, also published in [75]).

CHAPTER II

HIGH-FREQUENCY LOW-NOISE AMPLIFIER DESIGN AND CHARACTERIZATION

2.1 Power-Constrained LNA Design and Optimization

2.1.1 Introduction

Low noise amplifiers (LNAs) are a critical component in any receiver system, with stringent requirements for noise, gain, linearity, and power consumption. Emerging applications such as high-altitude radar systems and space-based radar systems, pose significant design challenges for receiver systems. The LNA requirements for these radars include: (1) very low-power consumption, (2) very low noise, (3) low cost per element, and (4) radiation tolerance.

The high altitude radar platform's limited power supply requires a receiver system with ultra low-power consumption. In receiver systems, LNAs can account for a large portion of dissipated power due to their near continuous operation. Low-power LNAs dissipating under 2 mW have been demonstrated in III-V technology [25], however, no low-cost silicon (Si)-based solution is currently available. A high-performance, ultra-low power LNA in a Si-based technology would allow for inexpensive and highly integrated receiver modules, clearly desirable for these high-altitude radar systems.

This section presents a summary of the work highlighted in [74]. This work presents the design of a low-power X-band LNA in SiGe technology, which achieves less than 2 dB mean noise figure (NF) while dissipating 2 mW of dc power. Section 2.1.2 outlines the LNA design procedure for low-power applications. Section 2.1.3 reports the measured results and comparisons against other state-of-the-art LNAs.

2.1.2 Design

The traditional inductively-degenerated cascode LNA topology, as shown in Fig. 10(a) is chosen here due to its power and noise matching ability. The design was accomplished through a modification of the process outlined in [41] with additional requirements to optimize for low-power dissipation. In the original procedure, the collector current density (J_c) is optimized for NF and gain. In order for the NF of the transistor to achieve NF_{min}, the optimum source resistance ($R_{s,opt}$) must be matched to the system impedance. The resistive component is set to the system impedance (in this case, 50 Ω) by scaling the emitter length. Thus, by matching the input to the system impedance, the noise impedance is simultaneously matched.

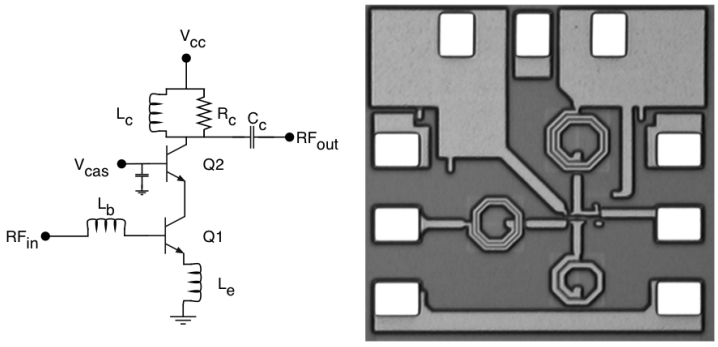


Figure 10: (a) Simplified schematic and (b) photograph of fabricated LNA

Scaling the emitter geometry to match the resistive component to the system impedance removes the need for a lossy matching network. $R_{s,opt}$, Eq. (5), and NF_{min}, Eq. (6), are given in [20], where L_E and W_E are the emitter length and width, respectively, $r_b \cdot L_E/W_E$ is the scaled base resistance, f is the operating frequency, f_T is the unity-gain cut-off frequency, J_c is the collector current density, β is the current gain, and g_m is the transconductance.

$$R_{s,opt} = \frac{f_T}{f}\frac{1}{L_E}\sqrt{\frac{2}{J_C}\frac{r_b L_E}{W_E}\frac{kT}{q}} \tag{5}$$

$$NF_{min} = 1 + \frac{1}{\beta} + \sqrt{2g_m r_b}\sqrt{\frac{1}{\beta} + \left(\frac{f}{f_T}\right)^2} \tag{6}$$

As can been seen from Eq. (5), $R_{s,opt}$ is inversely proportional to L_E, and therefore scaling L_E allows the selection of an optimum source resistance. It can also be shown that NF_{min} is independent of L_E, since the scaling does not alter the f_T at a fixed J_c. Therefore, NF_{min} is selected by biasing the transistor at optimum collector current density ($J_{c,opt}$), and then scaling L_E while maintaining $J_{c,opt}$ to achieve the desired source resistance. This methodology is not appropriate for low-power design since both J_c and L_E are selected independently, thus trading power consumption for NF and matching.

In this modified procedure, a fixed I_c is directly determined from the required power dissipation and supply voltage. In order to select the desired $R_{s,opt}$ and maintain this specified I_c, J_c cannot remain fixed as L_E is scaled. The fixed I_c requirement presents a trade-off since J_c, L_E, and $R_{s,opt}$ cannot be selected independently. To determine the optimum trade-off, NF_{min} and $R_{s,opt}$ are solved simultaneously, appropriately scaling J_c and L_E to achieve the desired I_c.

Fig. 11 shows simulated results for NF_{min} and $R_{s,opt}$ versus L_E for a fixed I_c = 1.33 mA. To achieve $J_{c,opt}$ for I_c = 1.33 mA, L_E must be 7.8 μm yielding an NF_{min} = 0.73 dB. However, for this emitter length, $R_{s,opt}$ = 250 Ω which severely degrades the input noise match. An $R_{s,opt}$ of close to 50 Ω is desirable in order to achieve a simultaneous power and noise match. By trading-off 0.3 dB NF, $R_{s,opt}$ is reduced to 75 Ω, yielding a more acceptable match.

If I_c is not fixed for low power operation, using the original methodology, $J_{c,opt}$ = 1.20 mA/μm^2, NF_{min} = 0.73 dB, optimum emitter length = 52 μm, and $I_{c,opt}$ = 7.5 mA. Therefore, an almost 6$\times$ savings in *dc* power consumption is achieved by using the modified methodology, while only degrading NF_{min} by 0.3 dB, a favorable tradeoff for these power constrained applications.

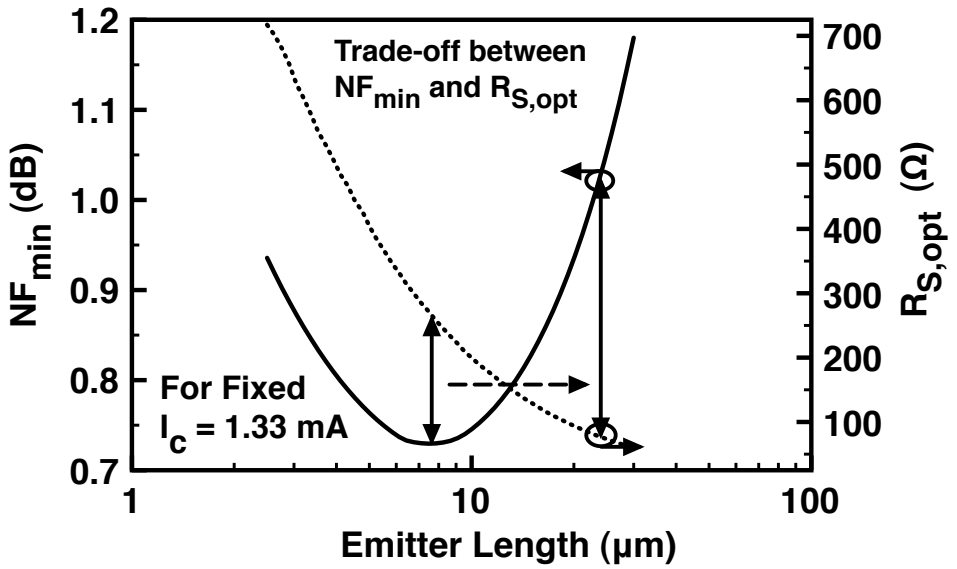


Figure 11: Simulated NF_{min} and $R_{S,opt}$ as a function of emitter length for a fixed I_c = 1.33mA.

The final total emitter area for this LNA was determined to be 0.12 μm $\times$ 24 μm. Due to process constraints, two 0.12 μm $\times$ 12 μm parallel devices were used. In order to maximize linearity and minimize power dissipation for both Q_1 and Q_2, V_{CB} for Q_2 was fixed at 0 V. The input matching network consists of base and emitter inductors. The emitter degenerative inductor matches the real part of the input impedance, while, the base inductor resonates out the base-emitter capacitance, C_{BE}. The output matching was realized through a shunt-RL, series-C passive network.

The design and simulations was performed using Cadence and Agilent's Advanced Design System (ADS) tools in a commercially-available 130 nm SiGe BiCMOS technology which includes a high-speed SiGe HBT with an f_T/f_{max} of 200/250 GHz, and a full suite of passive components [60]. Fig. 10(b) depicts the fabricated low-power LNA. The total area is 667 μm $\times$ 653 μm including bondpads.

2.1.3 Measured Results

2.1.3.1 Amplifier Characterization

The amplifier characterization was performed in an RF shielded room using an Agilent 8510C VNA and an ATN NP5B/Agilent 8970B system to measure scattering-parameters (SP) and broadband noise characteristics, respectively. Wafer-level calibration was performed to account for cable and probe losses. The two-tone linearity characterization was performed using two 8360 series swept signal generators and a 8563EC spectrum analyzer. Keithley 2400 source meter units were used to bias the LNA to V_{cc} = 1.5 V and I_c= 1.33 mA, yielding a total power dissipation of 2 mW.

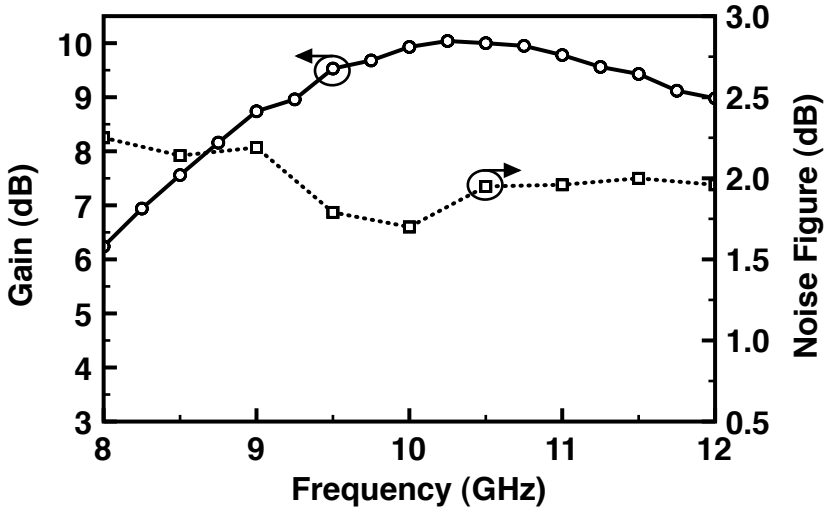


Figure 12: Measured gain and noise figure for the X-band ultra-low power LNA.

The two primary low-power LNA characteristics are shown in Fig. 12. The gain (S_{21}) is 10 dB at 10 GHz while the NF varies from 2.6 dB to 1.7 dB, yielding a mean NF of less than 2 dB. The -3 dB bandwidth is greater than 4 GHz, spanning 8.25 to 13 GHz needed for X-band radar systems (not shown). The return loss characteristics (Fig. 13) indicate a good match with both S_{11} and $S_{22} < -10$ dB at 10 GHz. The isolation is better than 45 dB over the entire band (not shown). In addition, the input third-order intercept point (IIP_3) is 0 dBm, using a fundamental of 10.00 GHz and a third order intermodulation term of 10.02 GHz (Fig. 14).

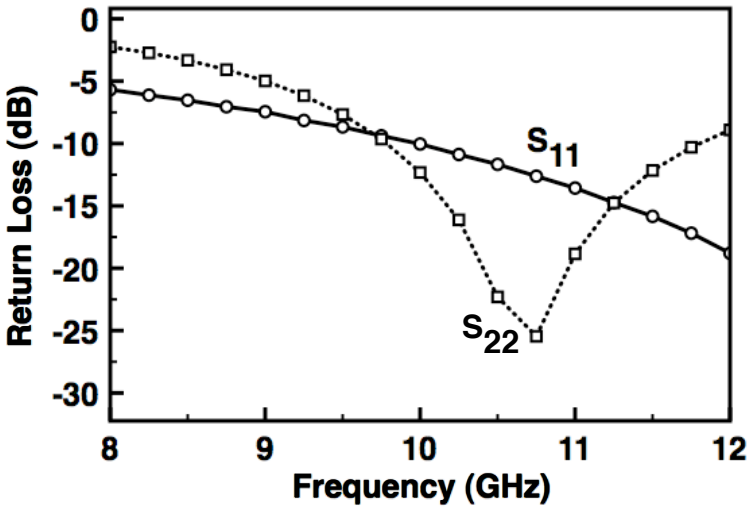


Figure 13: Measured S_{11} and S_{22} (return loss) for the X-band ultra-low power LNA.

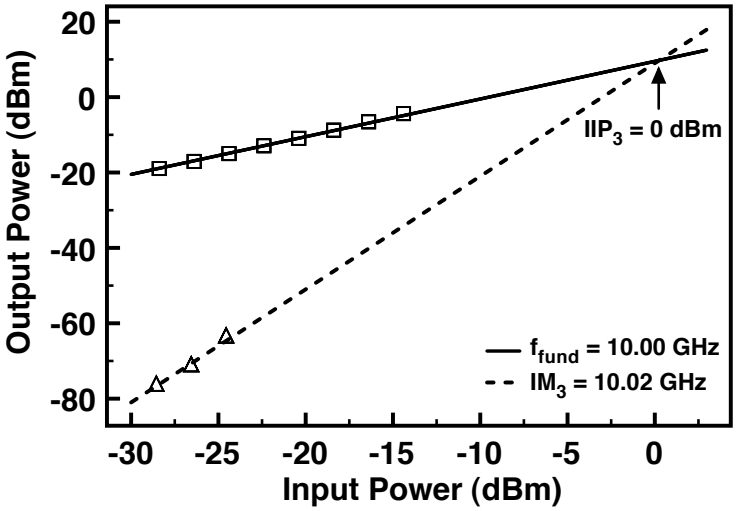


Figure 14: Measured input 3rd-order intercept point for the X-band ultra-low power LNA.

In order to perform an accurate comparison between various published LNAs, common LNA figures-of-merit (FOM) were calculated and benchmarked against the current literature. The first FOM, Eq. (7), measures the amount of gain achieved through one mW of dissipated power. The second FOM, Eq. (8), normalizes the gain by the NF and dissipated power. The final FOM, Eq. (10), accounts for the linearity and operating frequency of the LNA.

$$FOM_1 = \frac{S_{21}[dB]}{P_{diss}[mW]} \tag{7}$$

$$FOM_2 = \frac{S_{21}[mag]}{(NF[mag]-1)\cdot P_{diss}[mW]} \tag{8}$$

$$FOM_3 = \frac{S_{21}[mag]\cdot IIP3[mW]\cdot f_c[GHz]}{(NF[mag]-1)\cdot P_{diss}[mW]} \tag{9}$$

For all three LNA FOMs, a higher number represents better performance. Table 3 shows comparisons between 6 state-of-the-art LNA's operating at X-band. The LNA presented in this paper achieves the highest FOM of any Si-based LNA and is competitive with the FOMs for the existing antimonide-based compound semiconductor (ABCS) LNAs. The additional benefits of SiGe technology present significant cost, reliability, and yield advantages over an ABCS solution.

2.1.3.2 Radiation Response

A further facet of this low-power SiGe LNA's performance is its ability to withstand a large amount of total dose radiation, which is a needed qualification for extreme environment applications. The LNA was irradiated with space-relevant 63.3 MeV protons to proton fluences as high as 5×10^{13} cm^{-3}, at the Crocker Nuclear Laboratory at the University of California at Davis. The radiation and measurement setup has been previously described in [69]. Fig. 15 shows the LNA gain and NF response before and after a 6.7 Mrad dose proton radiation exposure. This radiation dose

Table 2: Comparison of ultra-low power LNA with other state-of-the-art LNAs

Reference	Frequency (GHz)	NF (dB)	Gain (dB)	P_{diss} (mW)	IIP_3 (dBm)	Technology	FOM_1 (dB/mW)	FOM_2 (mW^{-1})	FOM_3 (GHz)
This Work	10	1.98	10	2	0	200 GHz SiGe HBT	5.13	2.8	**28.07**
[40]	10	2.78	11	2.5	-9.1	180 GHz SiGe HBT	4.40	1.58	1.94
[41]	10	1.36	19.5	15	0.8	200 GHz SiGe HBT	1.30	1.71	14.23
[24]	8.2	1.6	22.0	14.4	-	70 GHz SiGe HBT	1.53	1.96	-
[25][1]	10	1.25	22.3	3.2	-	ABCS InAs/AlSb HEMT	**6.96**	**12.21**	-
[45]	0.3-11	1.2	16	5	-4	ABCS InAs/AlSb HEMT	3.2	3.96	3.15

[1]two-stage

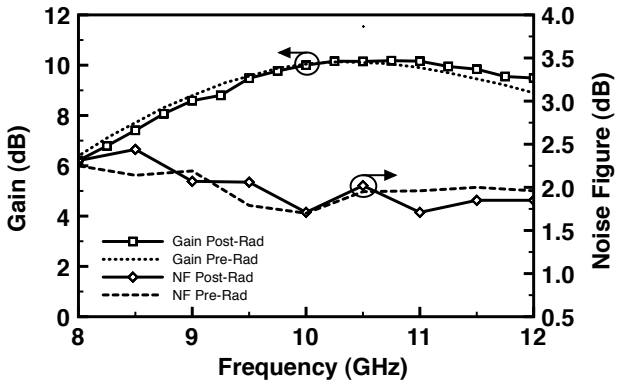


Figure 15: Measured gain and noise figure of the pre- and post-irradiation samples for the X-band ultra-low power LNA.

is more than an order of magnitude larger than what is typically experienced in low-earth orbit, and thus can be considered worst case. The post-irradiated sample shows almost no performance degradation. These results are consistent with the general understanding that SiGe HBTs are inherently total dose radiation tolerant as fabricated [17].

2.1.4 Summary

This section presented the design and characterization of a low-power X-band LNA achieving less than 2 dB mean NF while dissipating less than 2 mW of dc power, which can be used in advanced T/R modules for extreme environment applications. The LNA was designed using a modification of the typical inductively-degenerated cascode design technique. This technique allows the optimization of LNA design given a fixed power consumption constraint. A compromise between minimum NF and matching conditions was determined to optimize the LNA's performance. The designed LNA has a mean NF below 2 dB, a gain at 10 GHz of 10 dB, and an IIP_3 of 0 dBm. In addition, the LNA is radiation tolerant as fabricated, due to natural immunity of SiGe HBTs to total dose radiation. Benchmarked against other state-of-the-art LNAs, this SiGe LNA achieves the highest FOMs compared with other

Si-based LNAs, and is also competitive with current ABCS LNAs. This LNA is well-suited for new applications such as high-altitude and space-based radar systems, and highlights the potential of using SiGe technology to develop the next generation of low-power density phased array radar systems without compromising cost or performance.

2.2 Design of a High Dynamic Range X-band SiGe Low-Noise Amplifier

2.2.1 Introduction

In the previous section, the design of a power-constrained LNA targeting low-power applications was presented, however, another very important metric for LNA design is dynamic range. Dynamic range in an LNA is typically affected by system noise figure, intermodulation distortion (IMD), phase noise and bandwidth. Designing a high dynamic range (HDR) LNA continues to be challenging due to the requirements for: (1) low noise, (2) high gain, and (3) low power consumption. LNAs have a strong impact on the dynamic range performance since they contribute strongly to the system noise figure (driving noise and gain performance) while the LNA linearity will also impact intermodulation distortion, as measured by third-order intercept (TOI).

The HDR SiGe LNA was designed to achieve 30 dBm of output TOI, greater than 30 dB of gain, and less than 2 dB noise figure. Due to these demanding requirements, both a small-signal and large-signal amplifier design methodology was used to design the HDR LNA. The LNA was fabricated in a third generation SiGe BiCMOS platform (IBM 8HP). My specific role in this research was to design the first stage LNA, assist with final integration, and perform the on-wafer characterization.

2.2.2 LNA Design

The X-band HDR SiGe LNA was designed using a hybrid approach, considering both small and large-signal effects. For the desired output TOI (OTOI) of 30 dBm, using a common rule of thumb, an input 1-dB compression point (P1dB) of approximately 20

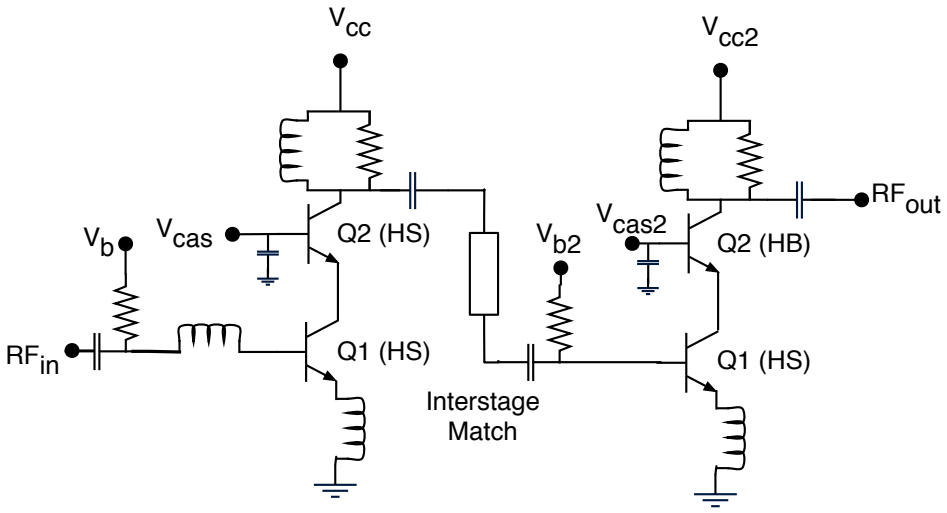


Figure 16: Schematic for two-stage HDR LNA with noise-matched first stage and power-matched second stage.

dBm is required, a value typically in the range of a PA, not LNA, design [3]. However, the stringent noise requirements require careful noise matching at the input to achieve a noise figure of less than 2 dB. In order to meet these conflicting requirements, a two-stage LNA was selected, the first stage designed as a inductively-degenerated cascoded LNA, as discussed in [41], while the output stage was designed as a PA utilizing both high-speed and high breakdown devices to maximize output power and swing [3]. To reduce the impact of noise generated from the second stage, the first stage provided 20 dB of gain, while the second stage was designed to have only 10 dB of gain. A degenerating inductor was also added to the second stage to improve matching and reduce gain while improving both linearity and noise performance. The inductive degeneration provides local negative feedback which decreases IMD levels, as discussed in [21]. A schematic highlighting the two-stage LNA is shown in Fig. 16.

For the first stage of the LNA, 0.12 x 10 x 3 μm^2 high-speed SiGe HBTs were selected, with a total current of 16 mA from a 2.5 V supply. In order to ensure gain flatness and high linearity across the desired bandwidth (8.5 - 10.5 GHz), the center frequency of the first stage was designed for over 10 GHz, while the center frequency for the second stage was offset to 9.5 GHz. For the core SiGe HBTs of

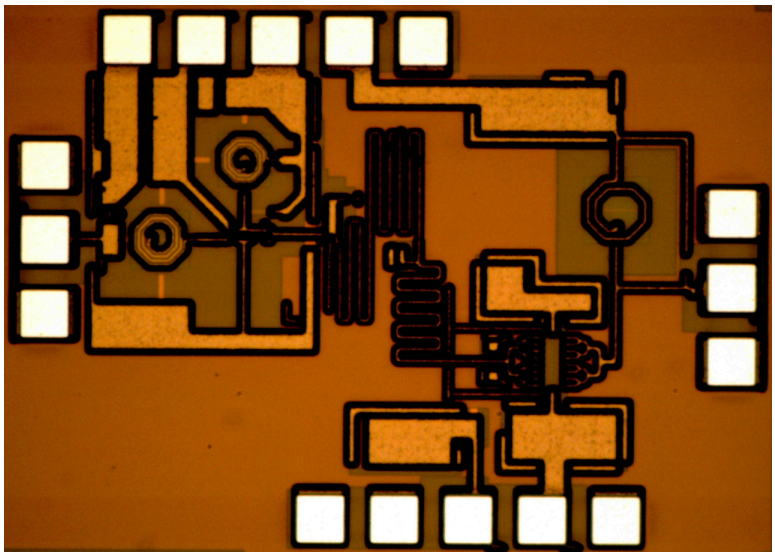


Figure 17: Micrograph of the fabricated two-stage SiGe HDR LNA.

the second stage, a novel high-performance / high breakdown cascoded structure was used to maximize large-signal performance. The high-performance common-emitter transistor was sized to 0.12 x 18 x 8 and the cascoded device was a custom-built (and modeled) high-breakdown 0.6 x 18 x 8 device, with total quiescent current of 48 mA from a 5 V supply.

The two-stage LNA, shown in Fig. 17, was fabricated in a 130 nm SiGe BiCMOS technology with seven metal layers and a full suite of mmW-passive components. The total area is 1.6 x 1.1 mm^2 including on-chip matching networks and bondpads.

2.2.3 Measured Results

The amplifier characterization was performed in a custom-built integrated S-parameter, noise figure, and load-pull on-wafer probing station designed in partnership with Agilent Technologies, Focus Microwaves, and Suss Microtech. I assisted in the system design, measurement methodology, and final system verification testing during the purchase and acquisition of this system at Georgia Tech. This station allows for single probing of the circuit with RF switching between the network analyzer, signal sources, and spectrum analyzer to conduct all RF and *dc* characterization without

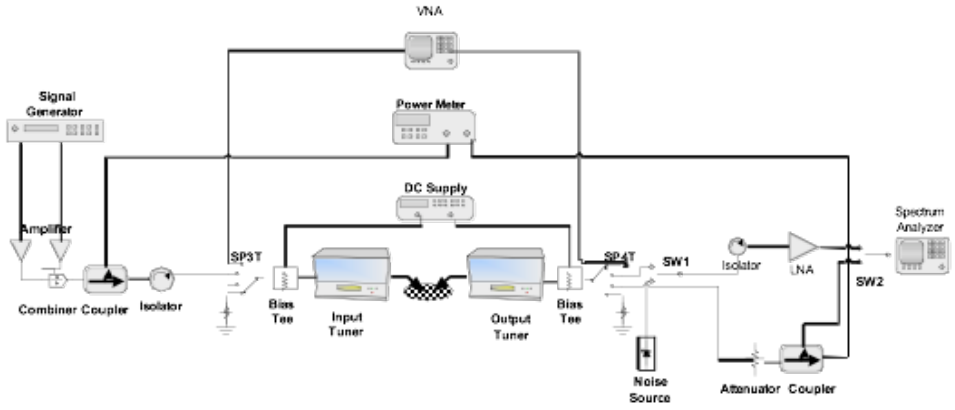


Figure 18: Diagram of custom-designed integrated S-parameter, noise figure, and load-pull station (Courtesy of Focus Microwaves).

modifying the measurement setup. A system diagram is shown in Fig. 18. The tuners, switches, and RF components are mounted on a Suss Microtech PM-8 probe station with probe shield technology providing RF shielding to the DUT.

The S-parameters are measured with both tuners initialized and the input and output switches are configured to the "VNA" setting, connecting the DUT to the Agilent E8363B PNA. Noise figure is measured with the switches configured for the noise receiver and noise figure is computed using the "cold-out" method (as discussed in [84]). The noise power is measured using the noise figure option of the Agilent E4446A spectrum analyzer. One-tone and two-tone measurements are then made by switching to the load-pull setting using two Agilent E8257D signal generators and the spectrum analyzer. All switching controls, instruments, and tuners are controlled via the Focus Load-Pull Explorer software. This system allows for high-accuracy and repeatability since all measurements were conducted within the same probe contact, bias condition, and measurement setup.

The measured S-parameters for the SiGe HDR LNA are shown in Fig. 19. The S_{21} of the LNA shows greater than 30 dB of gain, with over 2 GHz of bandwidth, and a gain flatness of better than $\pm$ 0.5 dB across band. The inset in Fig. 19 highlights the input and output return loss, with the input return below -15 dB across band,

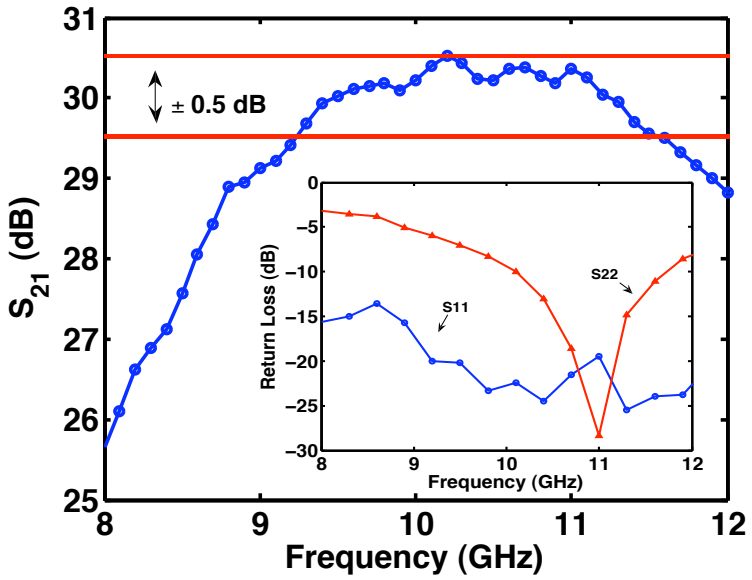


Figure 19: The gain (S_{21}) of the SiGe HDR LNA highlighting ± 0.5 dB of gain flatness with the inset showing the measured input and output return loss.

which is required to prevent a high-VSWR towards the antenna element.

The noise figure of the SiGe HDR LNA was determined by measuring noise power at 11 impedances and computing F_{min}, Γ_{opt}, and R_n. Fig. 20 depicts the 50 Ω noise figure results showing 2 dB of noise figure between 8.5 - 10.5 GHz. For 9.5 GHz, F_{min} = 1.89 dB, Γ_{opt} = 0.16 ∠ 33 °, and R_n = 16.2 Ω. The inset in Fig. 20 plots the noise circles starting from 2 dB, in 1 dB steps. The LNA is well noise-matched, as evidenced by the center of the noise circles located near 50 Ω. In addition, the noise figure remains under 3 dB even for input mismatches up to 3:1 VSWR.

The linearity of the LNA was measured at three fundamental tones, 8.5, 9.5, and 10.5 GHz with an offset of 10 MHz. Fig. 21 plots the TOI performance over frequency yielding a peak TOI of almost 30 dBm. The inset in Fig. 21 plots the fundamental tone output power at 9.5 GHz and the lower order IMD product at 9.49 GHz, with extrapolation of these curves showing the intercept point. At 9.5 GHz, the output TOI is over 29 dBm with 30 dB of gain, yielding an input TOI of -1 dBm. In addition to two-tone linearity measurements, single tone swept power

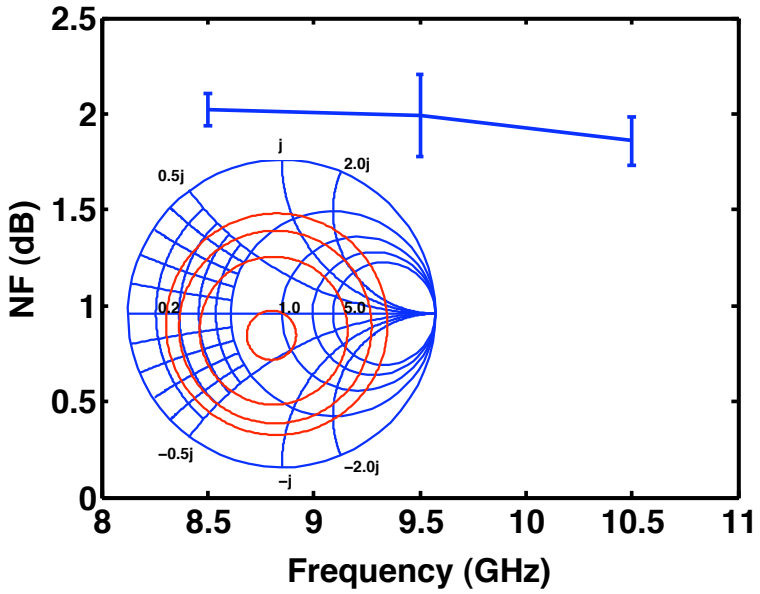


Figure 20: Measured 50 Ω noise figure of the SiGe HDR LNA at 8.5, 9.5, and 10.5 GHz with error bars highlighting measurement uncertainty and inset depicting calculated noise circles at 9.5 GHz.

measurements were conducted to measure the P1dB for the HDR LNA. The output P1dB was determined to be 18.5 dBm at 9.5 GHz, as shown in Fig. 22. A summary and comparison of the measured HDR LNA specifications is shown in table 3.

Table 3: Comparison of SiGe HDR LNA with Other X-band LNAs

Reference	Frequency (GHz)	NF (dB)	Gain (dB)	P_{diss} (mW)	OTOI (dBm)	OP1dB (dB)
HDR LNA	9.5	2.0	30	285	29	18.5
[41]	10	1.36	19.5	15	20.3	10
[32]	28	1.9	21	70	20	10
[12]	6	2.7	10.8	540	22.8	
[91]	6	1.6	10.9	120	23	13
[31]	8.5	0.53	32	109	20.5	10.5
[74]	10	1.98	10	2	10	0

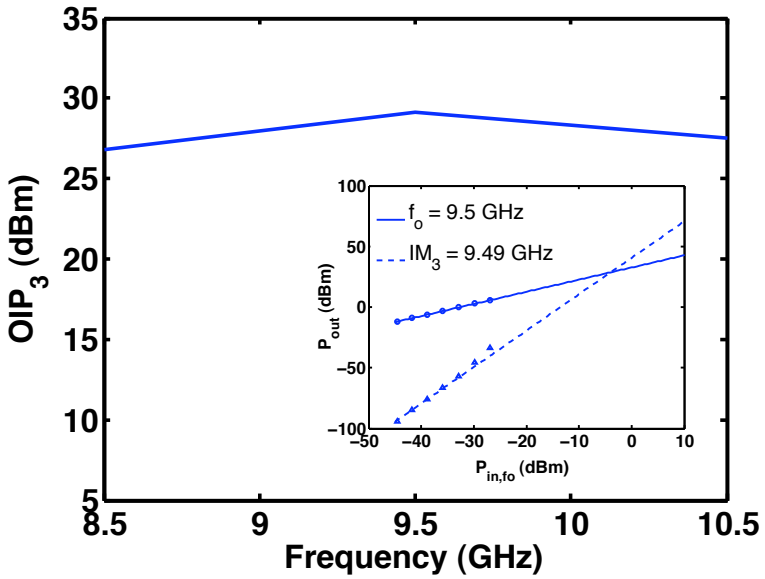


Figure 21: Output TOI of the SiGe HDR LNA using the lower side IMD product at 10 MHz spacing with inset highlighting measured and extrapolated TOI point at 9.5 GHz.

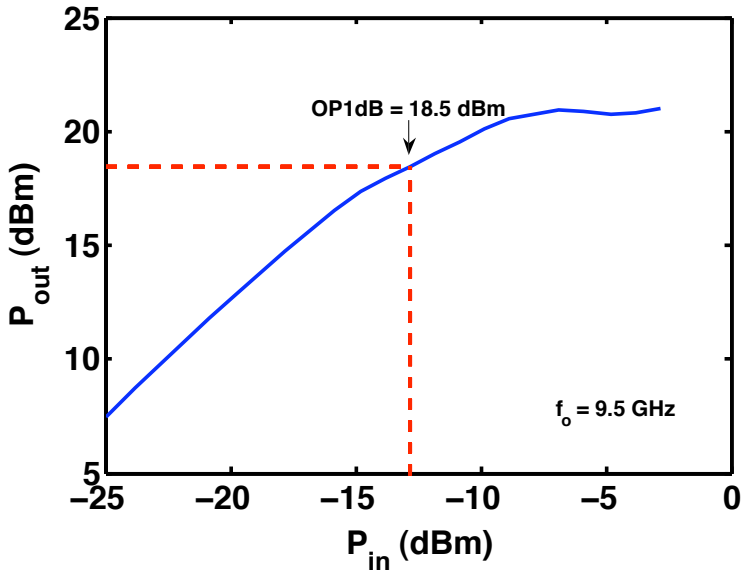


Figure 22: One-tone swept power of the SiGe HDR LNA at 9.5 GHz highlighting output 1-dB gain compression point.

2.2.4 Discussion

In order to understand the system-level impact of using such a HDR LNA, its performance can be compared against other baseline LNAs using two methods of analysis. The first approach analyzes system-level spurious-free dynamic range (SFDR) by inserting the LNA in a typical RF front-end and analyzing the total system dynamic range. The second analysis approach provides a comparison using a figure-of-merit based on relevant amplifier performance metrics. This combined analyse demonstrates the LNA impact in the context of system-level performance and also benchmarks it's raw performance against other state-of-the-art LNAs in the current literature.

SFDR characterizes the level of signal ranges that can be achieved, from the noise floor to the maximum signal level causing distortion, as defined in [88]. For this SFDR analysis, an LNA and receiver block were cascaded and total SFDR for the chain was calculated. The typical receiver used in this example was simulated with 10 dB of gain. A high-performance hypothetical LNA with a gain of 20 dB, noise figure of 1.5 dB, and an output TOI of 20 dBm was compared with the present SiGe HDR LNA. Fig 23 plots the system SFDR in dB at 1 MHz bandwidth for both cases of the typical LNA and SiGe HDR LNA, versus the noise figure of the receiver. The HDR LNA shows improved SFDR for nominal receiver noise figures due to the increase in gain while still maintaing a high output TOI. For the HDR LNA, the SFDR remains over 70 dB even for receiver noise figures above 15 dB. Thus, for typical receivers, using this high-gain, high-linearity LNA would provide dynamic range improvements by reducing the noise impact of subsequent stages, clearly an advantage to system designers.

To effectively compare LNA performance with LNA designs presented in part 1, comparisons are made using a modification to the figure-of-merit (FOM) presented in [53]. The modified LNA FOM expresses the impact of noise figure, gain, P1dB,

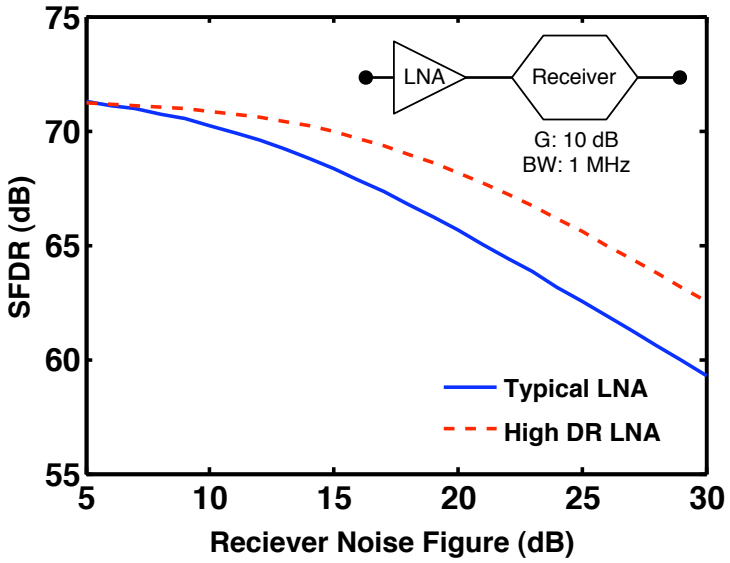


Figure 23: System spurious-free dynamic range (SFDR) as a function of receiver noise figure for the SiGe HDR LNA in a typical receiver system.

power consumption, and linearity on amplifier performance in the following manner:

$$FOM[dBm] = -NF[dB] + ITOI[dBm] + G[dB]$$
$$+10\log\left(\frac{P1dB[mW]}{P_{dc}[mW]}\right) + 20\log\left(\frac{f_o[GHz]}{1GHz}\right) \quad (10)$$

The inclusion of P1dB in this FOM emphasizes enhancements to the total available RF output power. The modified FOM includes effects of both small- and large-signal performance, which is more applicable for HDR LNAs. For this LNA, the FOM at 9.5 GHz was determined to be 39.5 dBm, which is greater than most comparable LNAs, even those fabricated in more costly III-V-based technologies. Table 4 highlights performance comparisons between seven state-of-the-art high-frequency LNAs.

2.2.5 Summary and comparison

The HDR SiGe LNA achieves 30 dBm of output TOI with a noise figure of 2 dB. The two-stage SiGe HDR LNA was designed using a hybrid design methodology, with the first-stage optimized for noise performance while the second-stage was optimized for linearity. The hybrid design technique of both LNA and PA analysis allowed for

Table 4: FoM comparison of SiGe HDR LNA with Other X-band LNAs

Reference	Technology	FOM (dBm)
HDR LNA	200 GHz SiGe HBT	39.5
[41]	200 GHz SiGe HBT	37.5
[32]	InGaP/InGaAs p-HEMT	41.6
[12]	AlGaN/GaN HEMT	21.1
[91]	GaN HEMT	29.1
[31]	GaAs mHEMT	28.7
[74]	200 GHz SiGe HBT	16.8

optimum LNA noise and linearity performance and helped provide additional TOI above typical SiGe HBT LNAs.

The design and optimization methodology for this design extends the traditional LNA design methodology as presented in part 1 of this proposal. The use of the PA output core as the second stage improves the linearity of the single-stage LNA, with a minimal increase in noise figure. By adopting this approach, a wide-band, practical high linearity amplifier can be designed by combining traditional LNA design and PA design techniques. By increasing linearity of the LNA, the overall system performance can be improved.

2.3 Large-Signal Robustness of SiGe HBT LNAs for High-Frequency Wireless Applications

2.3.1 Introduction

In the two previous sections, high-frequency SiGe LNA designs were presented, to conclude this chapter, this section explores the reliability of such LNAs operating in large-signal conditions. With the increased demand for high integration, reduced cost, and compact size in high-frequency circuits used in radar and wireless communication systems, circuit reliability becomes a major concern for system designers. Since highly integrated systems tend to increase the density of circuits and components, each module may contains many more elements, and a failure of any these components

would cause a failure of the module. Therefore, it is necessary to understand the reliability and degradation of each circuit block due to the various mechanisms of potential stress.

The RF front-end, and particularly the low-noise amplifier (LNA), is particularly susceptible to stress due to its required high input sensitivity and its exposure to the environment. In addition, if other components fail (such as a T/R switch), the full transmit power ($>$ 1 W) may be received by the LNA and therefore a single failed module can induce multiple failures [47]. To prevent damage, high-power limiters and other lossy components are typically added in front of the LNA; however, these components can greatly reduce system performance. Therefore, LNA robustness due to high levels of RF power is an important metric to help understand the reliability of larger, integrated modules.

In this research, I investigated the performance degradation of three different SiGe LNAs due to high-power RF stressing. Prior work has been reported on RF stressing SiGe PAs; however, this was conducted at lower power levels and higher voltages [10]. Both *dc* and *ac* perform metrics were measured before, during, and after stress to determine the effects of stressing on the circuit parameters. Section 2.3.3 describes the circuits measured and the measurement methodology, Section 2.3.4 presents the results of the high power stressing. Section 2.3.5 analyzes these results, and a summary is presented in Section 2.3.6.

2.3.2 LNA circuit description

Three different LNA variants were tested under high power RF stress. The first LNA (LNA_1) is the low-power X-band SiGe LNA discussed in section 2.1. LNA_2 was optimized for linearity and noise figure, and achieves a gain of 17 dB, with a noise figure of less than 1.5 dB, while LNA_3 was designed for higher gain (21 dB) and linearity. Both were based upon the design methodology highlighted in [41].

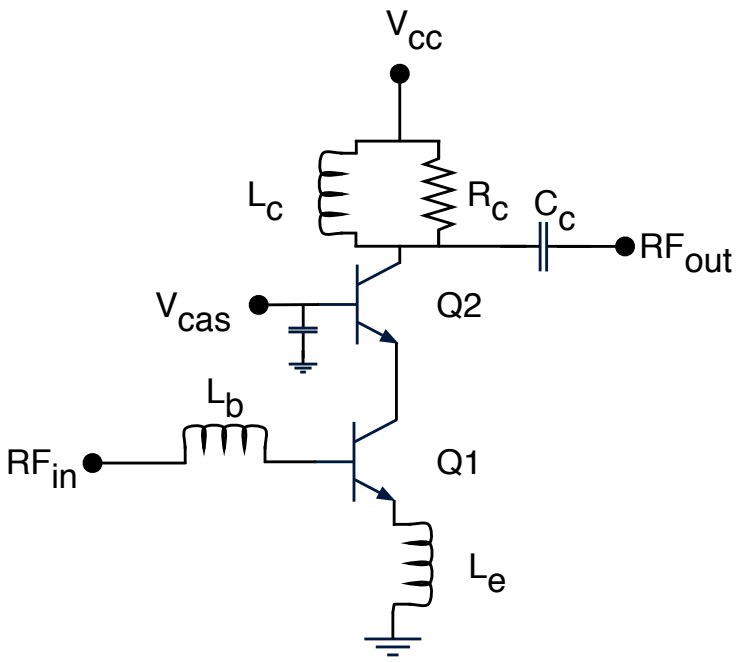


Figure 24: General inductively degenerated cascode topology for the X-band SiGe LNAs tested.

The general topology for all three amplifiers is shown in Fig. 24. LNA_1 was independently biased, requiring three separate supplies for the lower base, upper base, and collector nodes. $LNA_{2,3}$ contain an input *dc* block and are "self-biased," meaning that all the biasing was generated on-die from one supply voltage (2.5 V). The node-voltages are generated by a divider network and a HBT-based current mirror (not shown).

The LNAs were fabricated in a 0.13 μm SiGe BiCMOS technology (IBM 8HP). The SiGe HBT geometry in LNA_1 is 0.12 x 24 μm^2 while for $LNAs_{2,3}$ they are 0.12 x 30 μm^2. Die photographs of the LNAs are shown in Fig. 25.

In order to accurately determine the stress conditions for each LNA, characterization of the amplifier's compression point is first necessary to confirm that the applied large-signal stress is sufficiently high. For each LNA, the input power was swept from -25 to -7 dBm (Fig. 26). For all three LNAs, the compression point falls between -15 to -10 dBm of input power. Stressing at input powers over 25 dBm will be 35 to

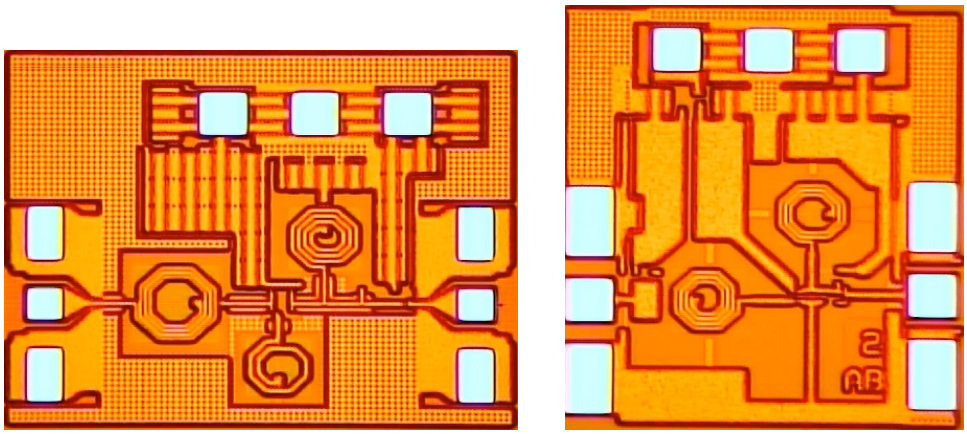


Figure 25: Micrographs of (a) LNA_1 and (b) LNA_2 (LNA_3 appears identical to LNA_2).

40 dB greater than the normal maximum signal, and should significantly stress the circuits, mimicking worst case scenarios.

2.3.3 Measurement Setup

The custom measurement setup allowed for accurate characterization of the pre- and post-stress performance is shown in Fig. 27. The general measurement methodology was to perform pre-stress measurements (Gummel characteristics and S-parameters), switch to the high-power path, apply large RF power (9.5 GHz CW tone) for specified time (400 sec), and then switch back to the VNA path to measure post-stress S-parameters and *dc* characteristics. During the measurements, the input/output power and circuit bias was recorded. The use of the RF switches allows the measurement to be performed *in-situ*, meaning that no change of the measurement setup is necessary to gather the pre- and post-stress data, ensuring high quality measurement. In addition, the entire setup was automated using Matlab. Finally, the impedance tuners allowed accurate 50 Ω response to be recorded and power data over impedance could also be measured.

The LNAs were measured on-wafer using high-frequency probes for the RF in/out, and *dc* probes to provide bias to the amplifier. Voltage and current sweeps using

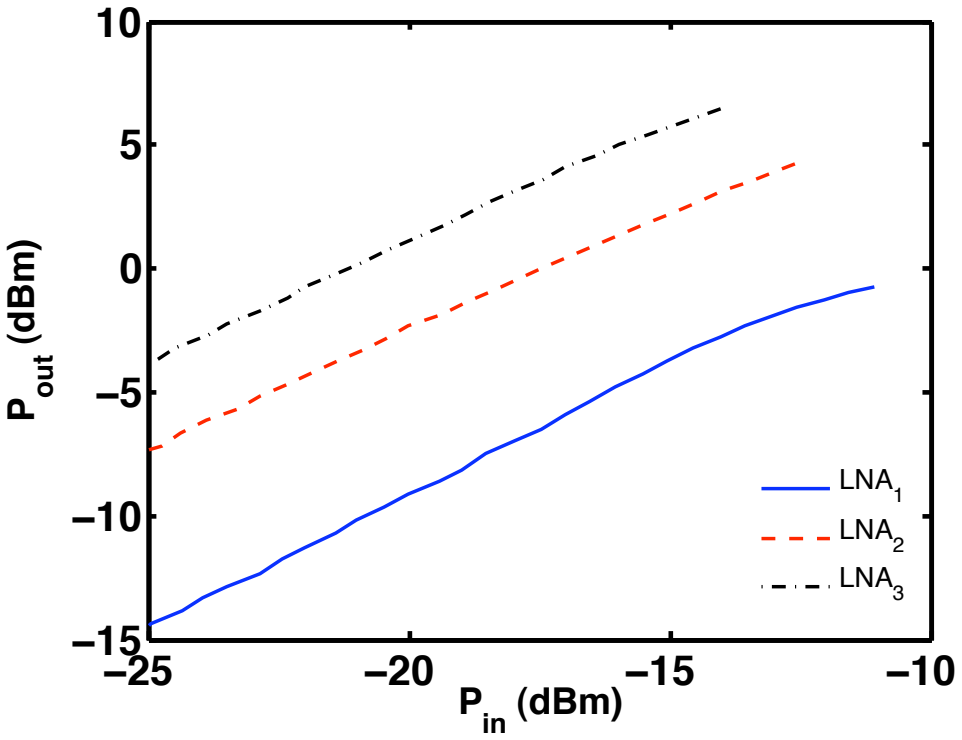


Figure 26: Swept power compression measurement for the three LNAs, highlighting input P1dB between -15 to -10 dBm.

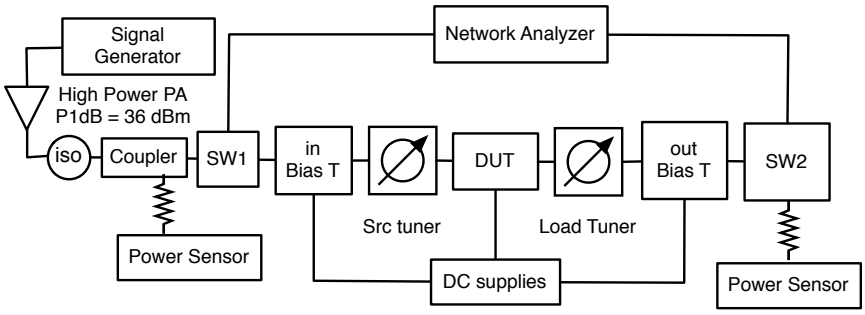


Figure 27: In-situ high power stress measurement setup which can provide up to 32 dBm of power to the device.

Keithley *dc* supplies were only performed on LNA-1 since it was independently biased and had access to all of the device terminals. A high power solid-state PA with 36 dBm P1dB (32 dBm maximum delivered to amplifier) provided the large signal for stressing the LNAs, and care was taken to avoid damage to the power sensors by adding 20 dB attenuators.

2.3.4 High power stressing results

Since LNA_1 was independently biased, the full *dc* characteristics before and after RF- stress were able to be measured. Typical degradation from stress should yield increase base leakage and degradation in current gain [94]. Fig. 28 plots the pre- and post-stress base and collector currents after applying 30 dBm signal to LNA_1. As expected, the base leakage at low-injection has greatly increased; however, the base and collector current at high injection was also reduced. In addition, the current gain (β) decreased to less than half its value from the pre-stress measurements. This large change indicates that significant damage is occurring in the devices. With 32 dBm of power applied, the LNAs suffered complete failure and therefore 30 dBm was used as the upper-bound for device stressing.

Even though the *dc* performance of LNA_1 was shown to greatly change during stress, the S-parameter performance does not exhibit quite as high degradation in performance (Fig. 30). The gain was shown to degrade by only a few percent at 30 dBm stress, and almost no degradation at 25 dBm stress as shown in Fig. 31.

For LNA_2, applying 30 dBm of stress caused the amplifier to fail, therefore a maximum power of 28 dBm was applied. Fig. 32 shows the difference in pre- and post-measurement gain stressed at 25 and 28 dBm. These results show a much higher degradation in gain over LNA_1, even though they are measured at lower power levels. For LNA_3, the amplifier did not fail with 30 dBm power, therefore, 28 and 30 dBm powers were applied. Fig. 33 exhibits an interesting result, where the 30 dBm level stress showed less degradation than with 28 dBm of stress.

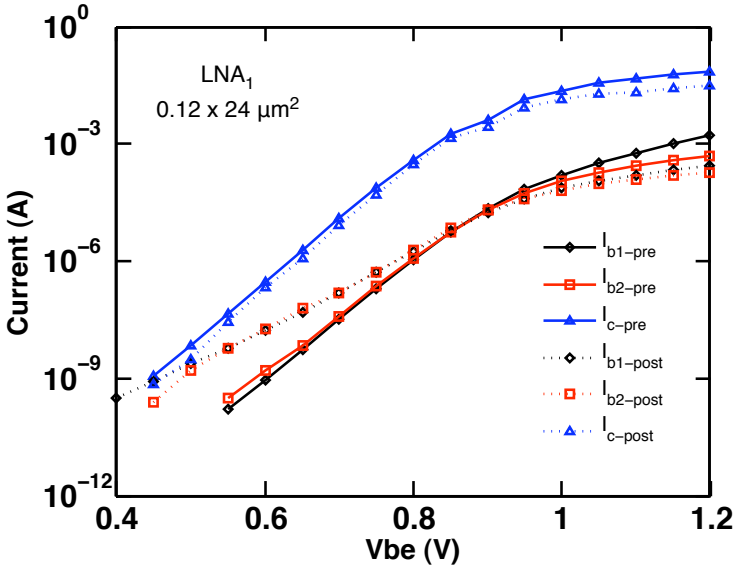


Figure 28: Gummel characteristic for LNA_1 before and after applying 30 dBm stress signal with noticeable degradation to I_{b1},I_{b2}, and I_c.

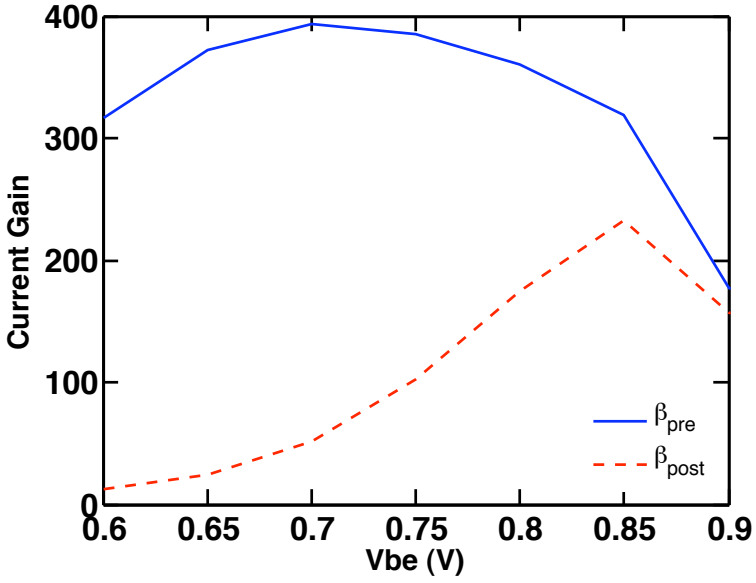


Figure 29: Current gain for LNA_1 before and after applying 30 dBm stress signal, highlighting over 2 $\times$ decrease in β.

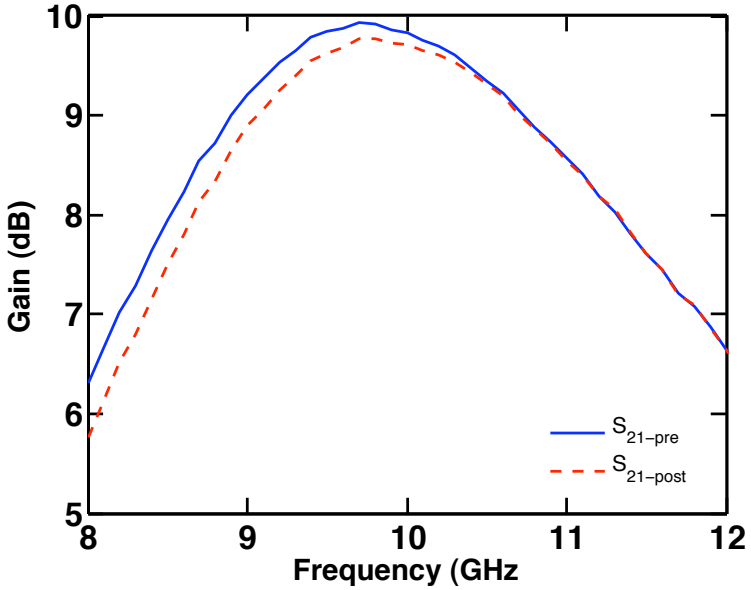


Figure 30: S-parameter results for LNA_1 before and after applying 30 dBm stress.

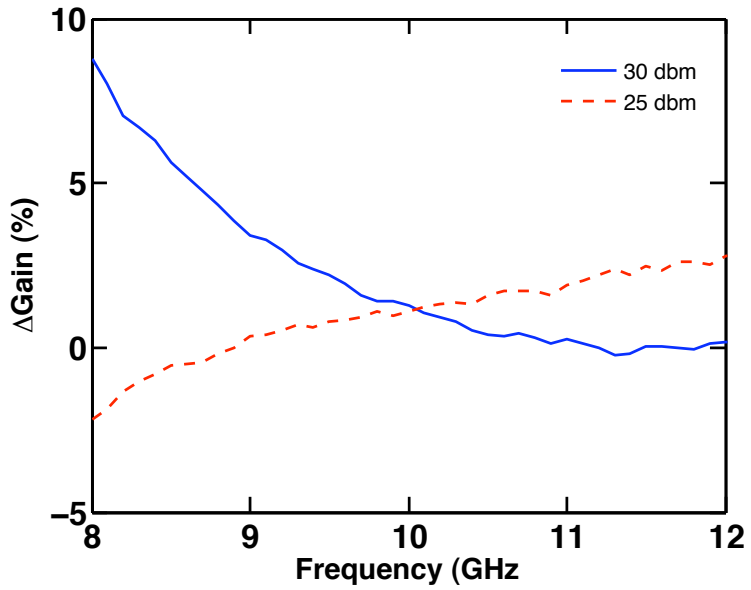


Figure 31: Change in gain for LNA_1 before and after applying 25 and 30 dBm stress.

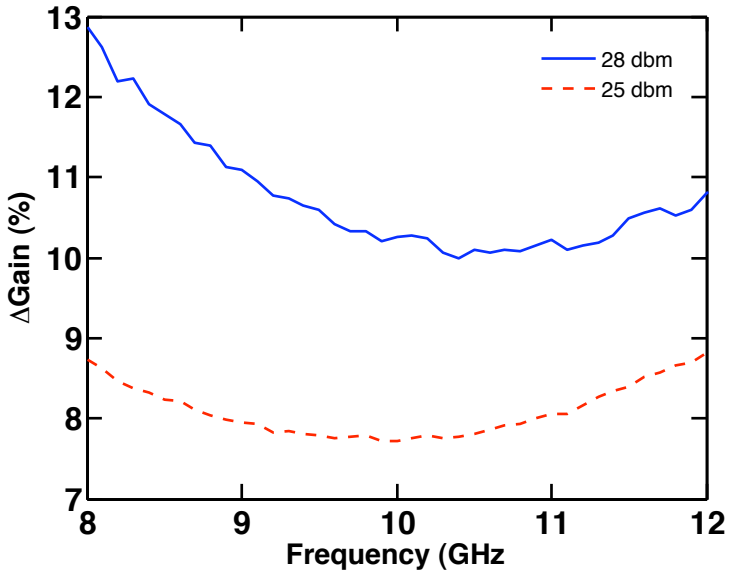


Figure 32: Change in gain for LNA_2 before and after applying 25 and 28 dBm stress.

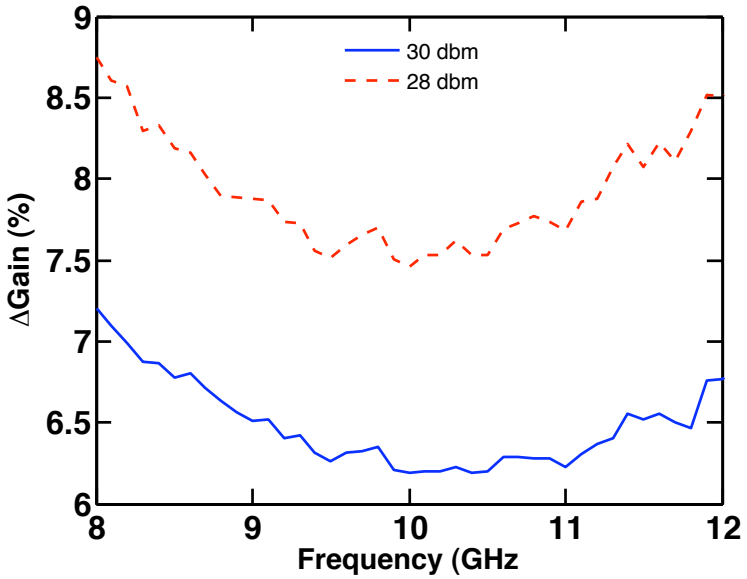


Figure 33: Change in gain for LNA_3 before and after applying 28 and 30 dBm stress.

2.3.5 Analysis

The measured results from these stress tests show that all three LNAs at these power levels, measurable performance degradation does occur. At powers at and above 30 dBm, complete failures can occur. Interestingly, levels of *dc* degradation may not necessarily translate into gain degradations as shown by LNA_1. The smaller level of gain degradation may be due to its lower operating voltage (1.5 V instead of 2.5 V). Traditional mixed-mode (simulataneous application of high current + high voltage) stressing directly relates to both voltage and current levels in the device [11], therefore, for the same current levels, a lower voltage device should yield less damage.

To better understand the damage due to RF stressing, the current densities during the applied RF power can be calculated. Fig. 34 plots these currents during the duration of the stress. These results show that the current densities are constant during the entire applied RF stress. Interestingly, LNA_1 which showed to have the lowest degradation, has the highest current density in for the maximum signal of 30 dBm. In addition, for LNA_2 and LNA_3, the maximum current densities are very comparable. However, for the LNA_3, the lower gain degradation might be due self-annealing effects which occur at very specific current densities as indicated in [11]. It is clear, however, that additional factors other than high current densities due to RF stressing contribute to determining circuit performance degradation. Applied voltage does appear to play a factor, but the differences in behavior between LNA_2 and LNA_3 cannot be fully explained by mixed-mode stress analysis. Therefore, further investigation into the damage mechanisms for high-power stressing of LNAs is needed to fully determine the sources of degradation, and are a subject of future research.

In addition to 50 Ω measurements, RF performance over varying impedance was also measured before and after 30 dBm stress for LNA_1. For this stress measurement, LNA_1 was biased with a forced base current instead of forced base voltage to ensure accurate biasing during load-pull. Fig. 35(a.) shows the pre-stress gain

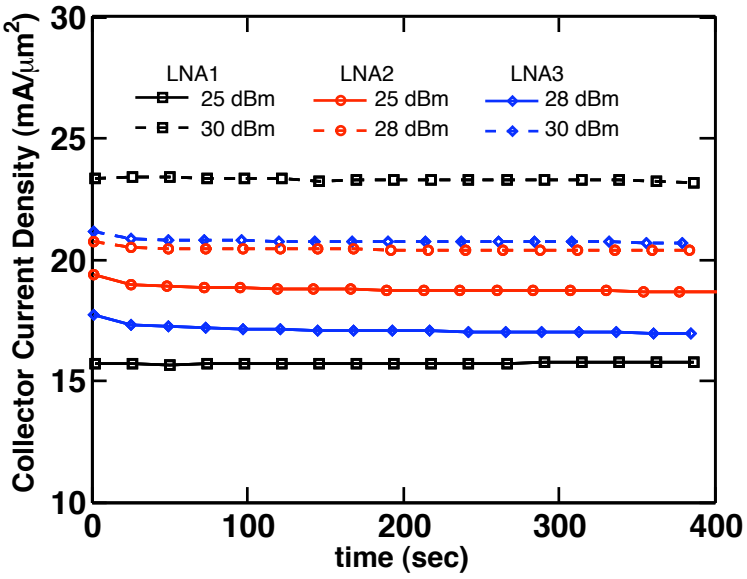


Figure 34: Dynamic collector current density during stressing of the LNAs.

over impedance, while Fig. 35(b.) plots the gain post-stress. There is a noticeable degradation and shift in peak gain. These results indicate that stressing does impact the transistor impedances and RF matching networks.

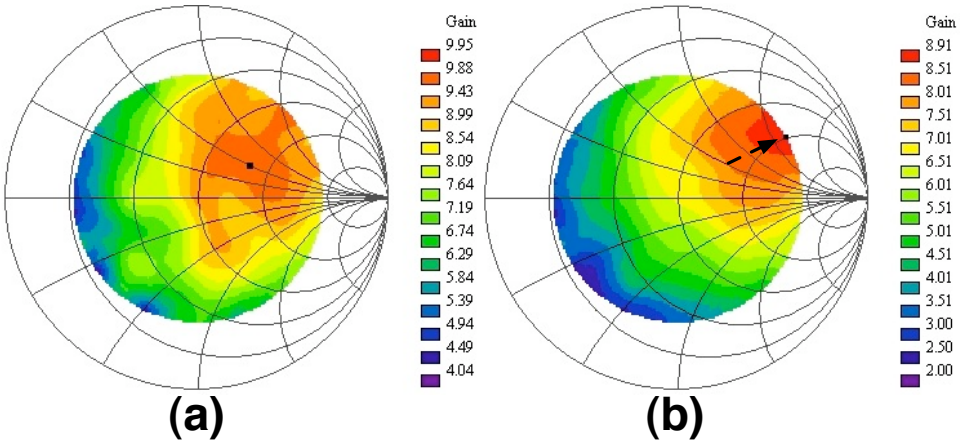


Figure 35: Load-pull results before and after 30 dBm of stress on LNA_1

2.3.6 Summary

This research reports the initial results of large-signal robustness testing of SiGe HBT LNAs. Three LNA variants were stressed, pre- and post-stress S-parameters were measured to determine circuit degradation. The custom measurement setup allowed for accurate high-power characterization and allowed in-situ stressing and measurement of pre- and post S-parameter results. At power levels at and above 30 dBm, failure in these LNAs was observed. In addition, *dc* characterization was performed on LNA_1 and indicate significant device damage does occur; however, they may not directly translate to degraded circuit performance. Previous work indicates that RF stressing acts as a "mixed-mode" stress; however, further investigation into these damage mechanisms are needed to explain the discrepancy between the degradation seen in all three LNAs. Finally, it was noted that device impedances do shift after stressing, indicative in changes to the transistor capacitances and resistances.

Further investigations are necessary in order to fully explain the observed damaage mechanisms, including characterizing the unmatched transistor cores, multiple samples, other LNA topologies, and load-pull measurements. However, from this investigation, it is clear that large-signal RF stressing of these LNAs do show significant damage and therefore, care should be taken to avoid exposing the RF front-ends to these power levels.

CHAPTER III

DESIGN AND IMPLEMENTATION OF ACTIVE PHASED-ARRAY RECEIVE ANTENNA

3.1 Introduction

Over the past few years, there has been an increasing desire to measure and characterize changes in the earth's climate, particularly, the accumulation and thicknesses of ice and snow cover. Obtaining data on the amount and makeup of ice and snow can aid scientists in developing better climate models and improve our understanding of climate change [27]. One example of this was NASA's Cold Land Processes Experiment (CLPX). This mission was to increase understanding of snow's impact on the hydrologic cycle and the climate. These studies used a combination of satellites, airplanes, and ground vehicles to measure snow cover, grain size, and freeze/thaw processes using radar systems [48, 67]. An example of a typical sled mounted radar system for monitoring of snow structure is shown in Fig. 36 as discussed in [48]. These systems can provide valuable insight into understanding snow depth and thicknesses, which can lead to a better understanding of climate phenomena.

Given the advances in low-cost RF and microwave technology over the past decade, future climate monitoring systems can be designed to be much smaller and lighter, with improved performance, enabling increased data gathering ability and, in turn, a better understanding of these climate phenomena. By targeting these next generation radar systems for platforms such as unmanned aerial vehicles (UAVs) coverage area would increase since these platforms can stay airborne for longer than manned airplanes.

As highlighted in Chapter 1 of this thesis, SiGe BiCMOS technology can be used in

Figure 36: Portable frequency-modulated continuous wave (FMCW) snow radar mounted on sled for measuring snow depth and ice thickness (from [48]).

order to meet cost, performance, and integration objectives, and is rapidly becoming a platform of choice for many radar system designers. Single chip SiGe T/R modules have been demonstrated to be suitable for use in these for active phased-array antennas systems; however, a multi-element antenna array using these components has not been demonstrated [15].

Another advance in microwave technology is the use of low-cost packaging solutions such as Liquid Crystal Polymer (LCP) and RXP. LCP enables high performance, low cost, compact size, high integration, and flexibility [8,22]. In addition, LCP can be processed using standard printed circuit board (PCB) manufacturing techniques [71], thus reducing the packaging and fabrication costs, which is typically a large portion of component cost. Combining these two technologies (SiGe + LCP) provides tremendous benefits, not only allowing the ability to create low-cost, sophisticated antenna arrays, but also allows smaller, highly-integrated, multi-element antenna arrays with the ability to mount on UAVs or other compact platforms. Current technology (III-V

+ inorganic package substrates, e.g., GaAs + Alumnia) are not only more costly, but also larger, power hungry, and are not suitable for large conformal arrays on compact platforms [6].

In this chapter, the first 8 x 8 element, X-band, active phased-array receive antenna array integrating 8 SiGe BiCMOS T/R modules on a multilayer organic (Duroid + LCP) antenna that includes a beamformer network and power combiner is presented. Section 3.2 and 3.3 discusses the phased-array antenna architecture and design of the SiGe T/R module, respectively. Section 3.4 presents the measured results of the receive antenna in a near-field range chamber. My role in this research was to design and test the SiGe T/R module, assist with testing the interface with the digital control, antenna assembly, and antenna near field range characterization.

3.2 Antenna Architecture and Design

The design of this system was performed in a top-down approach, where the application requirements and constraints drive component design decisions. The initial step was to determine the antenna array configuration and architecture requirements that were to be subdivided into smaller sub-array prototypes. For snow and cold land processing (SCLP), the center frequency was chosen to be 9.5 GHz, with 500 MHz of bandwidth [67]. The target platform was a UAV or other small aircraft, with the array mounted to the underside of the fuselage. The platform would execute level flight at an approximate altitude of 8 km, with the phased-array antenna scanning $\pm$ 20° port-to-starboard, resulting in swath coverage of approximately 6 km (Fig. 37).

To achieve sufficient directivity, a beamwidth of 2.2° in the scanned (X) direction is used. For the flight path (Y) direction, a smaller beamwidth of 0.8° is selected to provide both better resolution of measured ground returns and increased effective radiated power (ERP). Element spacing was chosen to prevent grating lobes, which

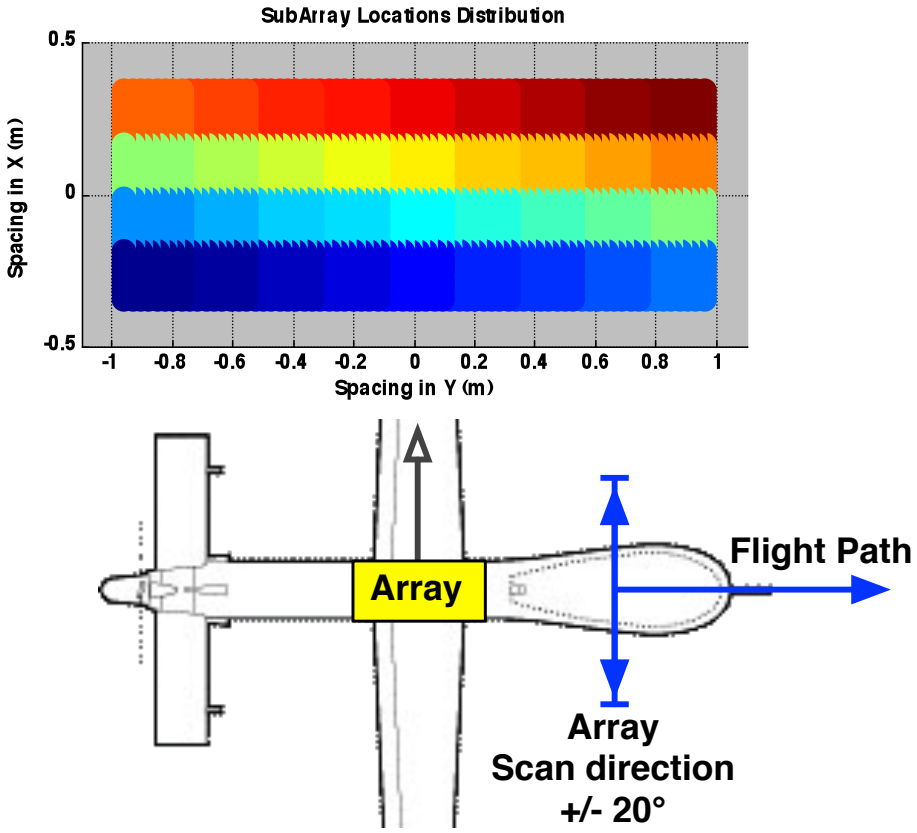


Figure 37: Proposed 2304 element radar system consisting of 36 (4 x 9) subarrays. Each subarray is comprised of 64 (8 x 8) radiating elements.

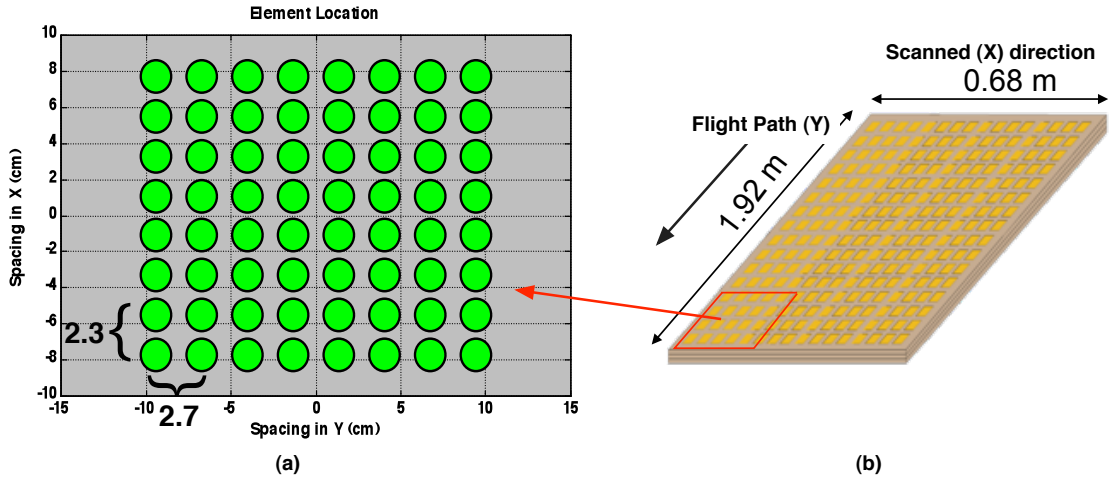


Figure 38: (a) Schematic of 8 x 8 subarray highlighting element space with total radiating area of 16 x 20 cm^2, (b) drawing of full antenna array with dimensions of 0.68 x 1.92 m^2.

are unintended beams (arising from spatial aliasing) that can degrade sensitivity.

$$\Delta s \leq \frac{\lambda}{1 + |\sin\theta_s|} \tag{11}$$

Eqn. 11 is used to calculate the inter-element spacing given a maximum scan angle of 20° at the maximum design frequency of 9.75 GHz. Given these dimensions, the spacing is 2.3 cm in the X direction and 2.7 cm in the Y direction as shown in Fig. 38 (a). Thus, the array size was determined to be 0.68 x 1.92 m^2 with 2304 radiating elements (Fig. 38 (b)). The large array is divided into 36 (4 x 9) subarrays, each containing 64 (8 x 8) radiating elements. The array presented in this chapter demonstrates a prototype receive subarray antenna element.

Antenna patterns derived from the 64 element subarray and full antenna are shown in Fig. 39 (a) and (b), respectively. As designed, the full array beamwidth was 2.2° x 0.8° for the full 2304 element array; the individual subarray possesses a beamwidth of 9.2° x 7.5°. In addition, the ideal antenna gains are 25.5 and 42.6 dBi for the subarray and full array, respectively. Based on these design decisions and a model of the backscattering coefficient of snow [83], an SNR of approximately 24 dB is

Table 5: Estimated Signal-to-Noise Ratio Calculations for Antenna Array.

G_r	Antenna Gain Receive	22.7 dBW
P_t	Peak Transmit Power	42.6 dB
G_t	Antenna Gain Transmit	42.6 dBi
λ^2	Wavelength (0.03 m)	-30.5 dB-m^2
σ	Radar Cross Section	9.8 dBsm
$(4\pi)^3$	Space loss factor	-33 dB
R^4	Range (8,000 m)	-156.1 dB-m^4
L	System Losses	-6 dB
N	Number of Pulses (128)	21.1 dB
	Signal Power	**-86.7 dBW**
F	Receiver Noise Figure	6 dB
k	Boltzmanns Constant	-228.6 dBWs/K
T	Thermal Temperature	24.6 dBK
B	Receiver Bandwidth (500 MHz)	87.0 dBHz
	Noise Power	**-111.0 dBW**
	SNR	**24.3 dB**

estimated, as shown in Table 5.

A phased-array antenna functions by introducing phase differences between the elements in the array as highlighted in Chapter 1 of this thesis. This action enables the beam to point in directions off broadside, i.e., electronic scanning. In order to increase performance, active phased-array antennas place transmit and receive amplifiers at the individual elements. As the antenna is only required to scan in a single direction, the elements on the subarray are divided into 8 x 1 array columns, with each column driving a single SiGe T/R module, as shown in Fig. 40.

Each radiating element is a slot-fed, aperture coupled microstrip patch antenna. The antenna is formed from three LCP (Rogers 3850/HT) layers and a Duroid (RT/Duroid 5880LZ) layer , with a stack up of the antenna shown in Fig. 41. This design utilizes two LCP layers consisting of 75 μm (50 μm core plus 25 μm bondply) and 100 μm thicknesses laminated to a 1.27 mm thick duroid layer using a 25 μm LCP bondply. Two bond ply layers (25 μm each) were needed for the multi-layer lamination, leading to a total thickness of 1.47 mm. Thin LCP layers were used to

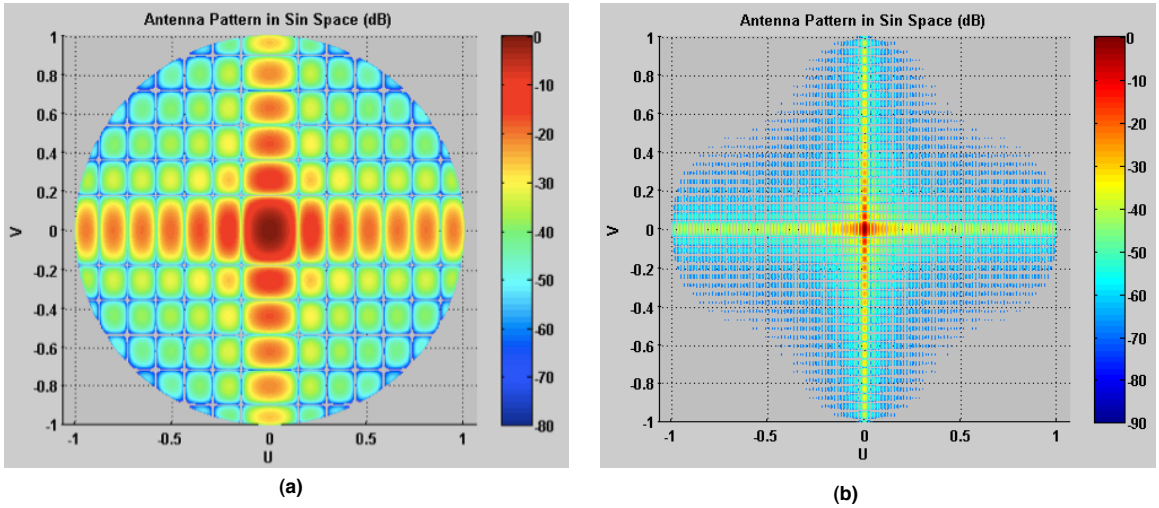


Figure 39: (a) Simulated ideal antenna pattern for 64 element, 8 x 8 subarray, (b) simulated ideal antenna pattern for full 2304 element array.

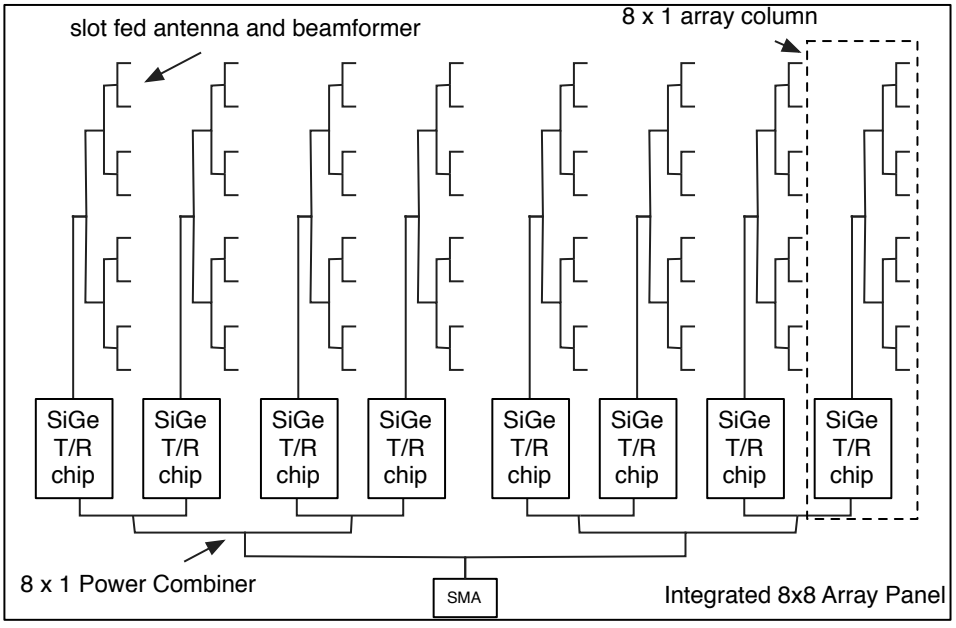


Figure 40: Topology of 8 x 8 subarray receive antenna array, showing slot-fed antennas, beamformer, SiGe chips, and power combiner.

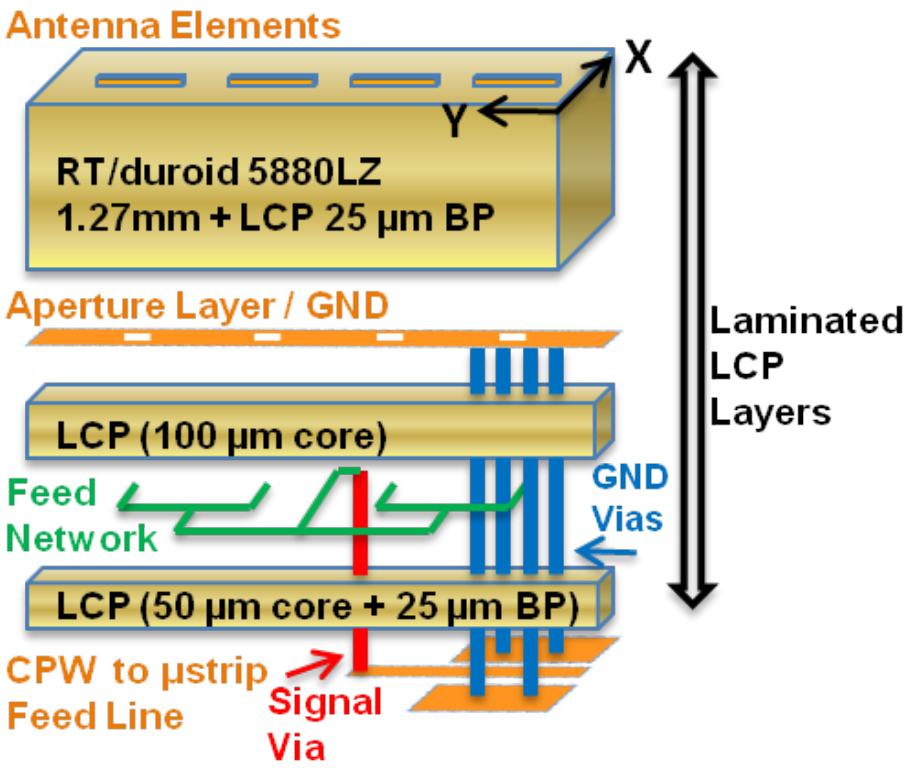


Figure 41: Stack up of multilayer 8x8 antenna array showing only one column with four elements.

limit radiation losses through the large feed network and a thicker Duriod layer was used to achieve the necessary bandwidth.

Each of the 8 radiating elements are combined using an equal division T-junction beamformer network, which is wire-bonded to the LNA input. In the final design, a MEMS T/R switch will be added to allow the array to switch between transmit and receive modes. Further details of the antenna design can be found in [61, 62]. Each of the 8 x 1 array columns are combined using an 8 x 1 equal distribution power combiner which is then connected to a single end-launch SMA connector. The 8 x 8 subarray, weighing 100 g (without cables, chips, and connectors), has a total active area of 25.4 x 18.4 cm^2.

3.3 SiGe T/R module

The T/R module is a critical component in active phased-array antenna systems, which provides higher antenna gain, increased radiated power, and phase-shifting capabilities. For this antenna sub-array, 8 T/R modules are used in receive mode to boost the gain through a low-noise amplifier (LNA) and phase shifters to provide beam steering in the azimuth direction. For the full 2304 element array, a total of 288 T/R modules (8 T/R elements per subarray x 36 subarrays) is required. Traditionally, high-performance T/R modules (based in III-V technology) are costly, large, and lack integration of analog, digital, and RF components on a single-chip, and therefore would not be suitable for this low-cost, integrated antenna array. This T/R module was fabricated in the commercially-available IBM 8HP SiGe BiCMOS process which contains 0.13 μm CMOS and a third-generation SiGe HBT with f_T/ f_{MAX} of 200/250 GHz [65]. The technology offers state-of-the art CMOS and SiGe HBT transistors, as well as thick analog metal layers, a full suite of passive elements, and standard digital library blocks, allowing design of true low-cost single-chip T/R module containing RF, analog, and digital blocks.

The integrated T/R module topology consists of an LNA, power amplifier (PA), T/R duplexer switch, 3-bit phase shifter, digital control, and bias references. For this work, only the receive path was characterized, with future work aiming to include a MEMS T/R switch to fully utilize both the transmit and receive functions. A block diagram of the single-chip T/R, highlighting the receive path, is shown in Fig. 42.

3.3.1 LNA design

The single-stage X-band SiGe LNA used in this design was based on the inductively-degenerated design topology highlighted in [41]. This technique achieves simultaneous gain and noise figure matching, optimizing the LNA performance. Using this technique, the LNA was measured to have over 16 dB of gain and less than 1.5 dB of

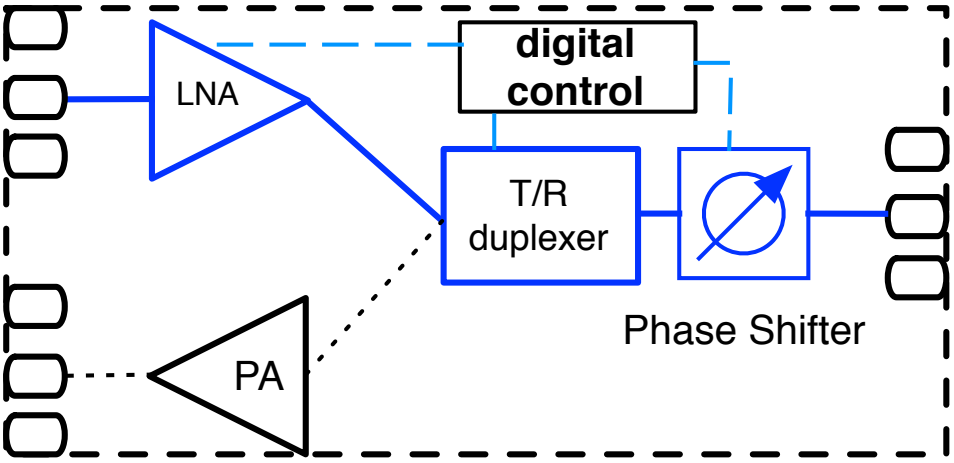


Figure 42: Block diagram of integrated SiGe T/R module, highlighting receive and digital control paths.

noise figure at 9.5 GHz with a 3 dB bandwidth of greater than 1 GHz with all RF matching performed using the on-chip passive elements.

In addition, bias control circuitry consisting of a band-gap reference (BGR) and CTAT current source was added to achieve process stable and robust operation. A schematic of the LNA circuit is shown in Fig. 43 The cascoded LNA requires three internal bias nodes, the upper collector at 2.5 V, upper base at 2.0 V, and base voltage at 860 mV. In order to achieve these voltages, the BGR and current source operate from a 3.5 V supply, with the BGR providing a stable 2.5 V. Details of the voltage reference design can be found in [55]. The voltage reference is used as the upper collector voltage and to create the 2.0 V for the upper base using a resistor divider network. The lower base is biased from a current source that supplies a stable 600 μA of current into a diode connected device (Q3), which is mirrored to (Q1). In addition, an LNA enable digital signal is used to bypass the current source, which allows the LNA to powered down.

The LNA including bias networks draws approximately 10 mA of *dc* current (35 mW of *dc* power), which is reduced to 1 mA in standby mode (3.5 mW). The ability for the LNA to enter standby serves two purposes: to improve chip efficiency during

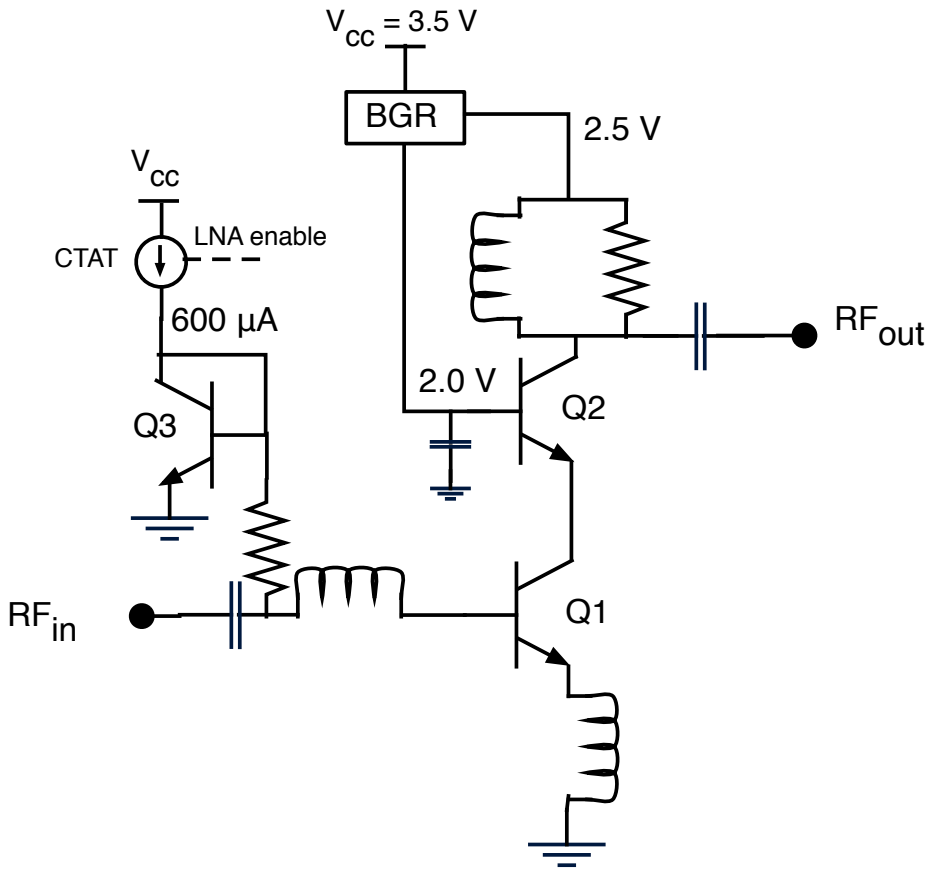


Figure 43: Schematic of inductively-degenerated X-band LNA with integrated bias references and digital control.

transmit mode and increase isolation between transmit and received signals. The LNA, including bias and matching networks, occupies less than 1 mm^2 allowing a highly compact and integrated design.

3.3.2 T/R duplexer switch design

In order for the phase shifter to be used for both transmit and receive paths, a T/R duplexer is used to switch between the LNA and PA, as shown in Fig. 42. The T/R switch is a triple-well nMOS series-shunt single pole double throw (SPDT) RF switch (Fig. 44). The series nMOS device serves as the "pass-gate" while the shunt nMOS device is added to improve the isolation. Triple-well series nMOS devices are used to improve insertion loss by floating the body and gate nodes, reducing the capacitive losses of the pass-gate device. This switch topology consumes almost no power, while achieving moderate insertion loss and isolation. Further details of the switch design are provided in [13, 79]. The source and drain nodes of the switch are biased to the same potential, and therefore no *dc* power is consumed by the switch. These bias voltages are generated by an on-chip bias network from a 3.5 V supply, which can be shared with the LNA, thus reducing the total I/O pad needed for the chip.

In order to improve isolation between the transmit and receive paths, an additional series device (M3) is placed in the PA switch path. Digital control circuitry is used to perform level shifting; and generate all T/R bit signals necessary to control both the switch and the LNA enable functions. The LNA path of the switch has less than 2 dB of loss while the PA path has slightly higher loss due to the additional series device added to improve isolation.

3.3.3 Phase shifter design

The final block in the receive chain is the 3-bit CMOS phase shifter. The phase shifter consists of hi-lo pass filter sections, which are switched using SPDT nMOS switches. The switches are similar to the topology of the T/R duplexer, with the exclusion of

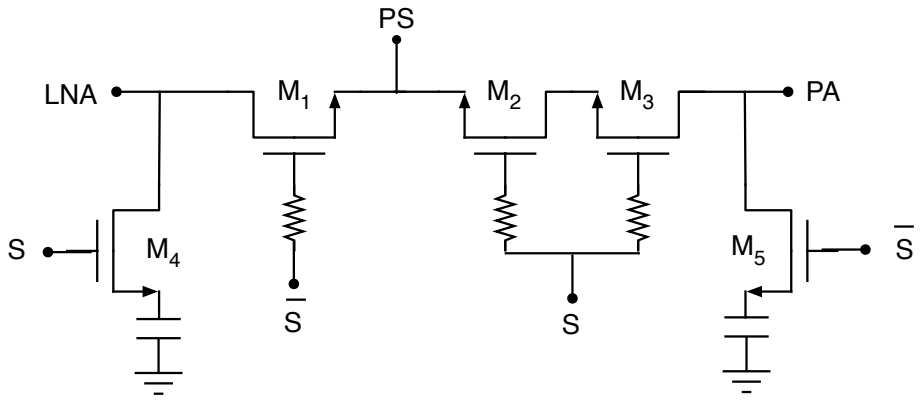


Figure 44: T/R duplexer SPDT switch schematic.

transistor M3. A matching inductor at the common port improves the return loss of the switch and enhances the RMS phase errors. Since each nMOS device is operated in a passive configuration ($V_{DS} = 0$), the device only draws leakage currents, with less than 1 μW power consumption for each switch. The total phase shifter has approximately 8 dB of loss. While active phased shifters, as discussed in [35], have less loss, they consume considerably more *dc* power and not well suited for power constrained applications, such as UAVs.

The schematic for the filter sections are shown in Fig. 45. Three sets of filter sections provide either 45, 90, or 180° differential phase shift matched to 50 Ω. Each hi-pass filter is designed to provide a negative phase shift, with the corresponding low-pass filter yielding a positive phase shift of equal magnitude, resulting in a phase difference between the two paths. The hybrid-*pi/t* filters provide a significantly more compact layout than traditional *pi* and *t* networks due to the reduced number of large inductors [51]. The filter sections were placed in the following order: 90, 45, 180, which provides the optimal ordering to reduce phase error and prevent loading from previous bits [52].

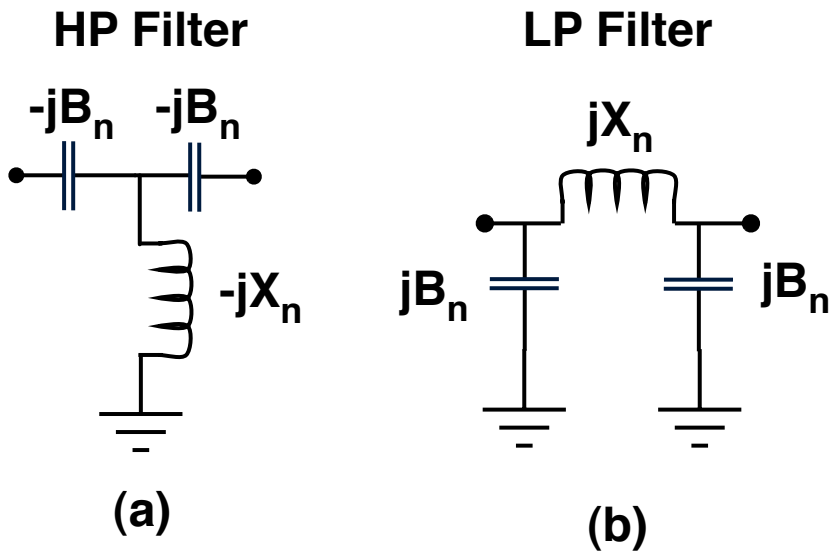


Figure 45: Hybrid hi-pass filter (a) and low-pass filter topologies where $B_n = tan(\Delta\Phi/4)$ and $X_n = sin(\Delta\Phi/2)$.

3.3.4 Digital control design

In order to control all 8 SiGe T/R modules in the 8 x 8 subarray panel, a VHDL beamsteering computer was designed to run on a Spartan 3A DSP 1800 evaluation board. Xilinx tools were used for the FPGA development including the Embedded Development Kit (EDK). The EDK is used to implement a Microblaze microprocessor on the FPGA, which is a RISC processor IP core developed by Xilinx. The processor is programmed in 'C' and is used to store phase shifter states. It also provides a command line interface (CLI) for users. Communication with the Microblaze is performed using serial RS-232 via HyperTerminal.

Each SiGe T/R module includes three phase bits, plus one common T/R bit; therefore, a total of 25 I/O digital control lines are needed. A serial-to-parallel converter is implemented on the SiGe T/R module; however, due to logic level differences, the deserialization was performed in the FGPA. For future designs, the on-chip serial-to-parallel converter with logic level translation will be used, reducing the number of digital I/O signals for the 8 x 8 subarray to only 4 (serial data, clock, latch, and

T/R), greatly simplifying board layout.

The beamsteering functionality is achieved by calculating the appropriate phase states (8 total states / phase shifter) for each of the 8 phase shifters in the subarray panel to achieve a specific scan angle. Scan angles were selected to allow full coverage over the ± 20°, with overlapping 3 dB beamwidths. Broadside (0°) and six other scan angles: ± 9.09, 18.19, and 24.21°, were selected; additionally angles of ± 32.86° were also calculated to observe the extents of the beamsteering and grating lobes. A phase shifter state table for all scan angles was programmed into the FPGA, which allowed simple beamsteering by simply selecting a specific scan angle and outputting the correct bit setting for each phase shifter.

In order to interface the I/O from the FPGA to the subarray panel, an EXP prototype card was mounted to the FPGA, a photograph of the FPGA and EXP board with pin headers is shown in Fig. 46. The software allows setting the scan angle and configuring all phase shifters in unison or controlling each of the phase shifters individually for debugging purposes.

3.3.5 Measured on-wafer T/R module receiver results

Before integrating the SiGe T/R module into the antenna array, on-wafer level measurements were conducted to verify operation of the SiGe chip. The die area is approximately 2.5 x 3.7 mm^2 as shown in the die photograph in Fig. 47. This layout was not space optimized since extra debugging bondpads were included to test the various circuit blocks, optimization should yield approximately 30% area savings.

The T/R module characterization was performed in a custom-built integrated S-parameter, noise figure, and load-pull on-wafer probing station, as outlined in [78]. The tuners, switches, and RF components are mounted on a Suss Microtech PM-8 probe station. This station allows for single probing of the circuit with RF switching between the network analyzer, signal sources, and spectrum analyzer to conduct

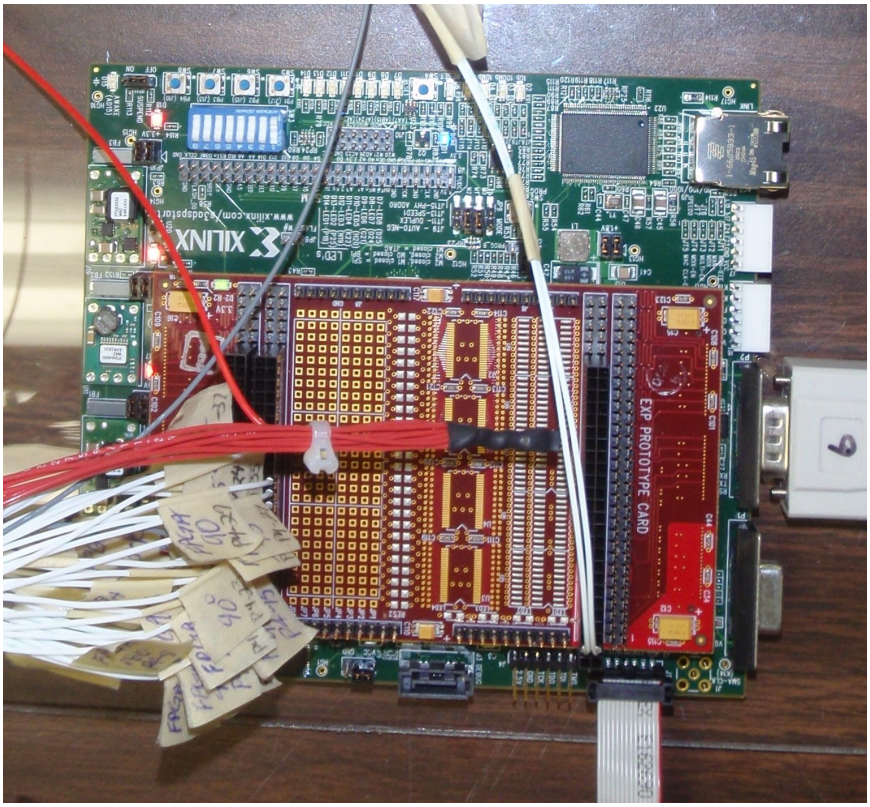


Figure 46: Photograph of FPGA and EXP board that are used for the beamsteering computer.

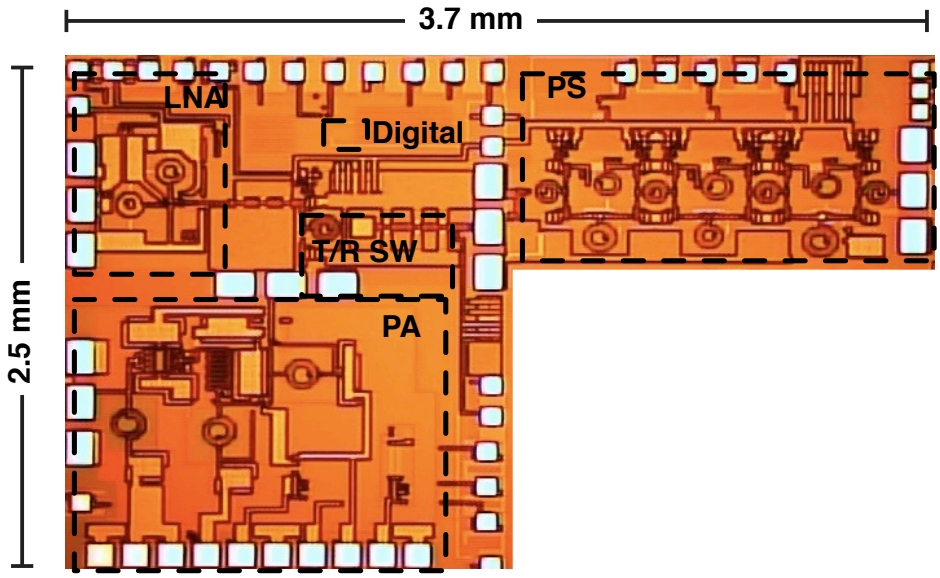


Figure 47: Die photograph of the integrated SiGe T/R module with outlines depicting the major circuit blocks.

all RF and *dc* characterization without modifying the measurement setup. The S-parameters are measured with the Agilent E8363B PNA. Noise power is measured using the Agilent E4446A spectrum analyzer and the noise parameters are extracted using the "cold-out" method (as discussed in [84]). One-tone and two-tone measurements are then made by using two Agilent E8257D signal generators and the spectrum analyzer. All switching controls, instruments, and tuners are controlled via the Focus Load-Pull Explorer software. This system allows for high-accuracy and repeatability since all measurements were conducted within the same probe contact, bias condition, and measurement setup. For the measurement of the T/R module receiver, the RF was probed on-wafer, while the *dc* and digital pads were bonded to a test fixture to provide biasing and control signals.

Measuring the S-parameters at each phase state yields the results shown in Fig. 48. The gain is approximately 7 dB at 9.5 GHz with less 1 dB of variation within the 500 MHz bandwidth and over all of the phase states. The phase is linear across frequency, with only a small deviation from the ideal phase. The input and output return loss (not shown) was measured to be better than -10 dB across the desired bandwidth.

The slight deviation in phase is due to an offset in the 180° bit. This can clearly be seen in Fig. 49, which plots the measured versus desired phase for all of the states at 9.5 GHz. The measured phase for the states using the 180° bit are slightly less than the desired phase, current design iterations of the T/R module have corrected this deviation in phase.

In addition to characterizing S-parameters over the phase states of the T/R module, the noise figure was also measured using the custom measurement setup. Fig. 50 shows both the minimum and 50 Ω noise figure of the receiver across frequency. The average noise figure in the 0° phase state across the band is approximately 2.5 dB, with only small deviations between the minimum and 50 Ω noise figure indicating

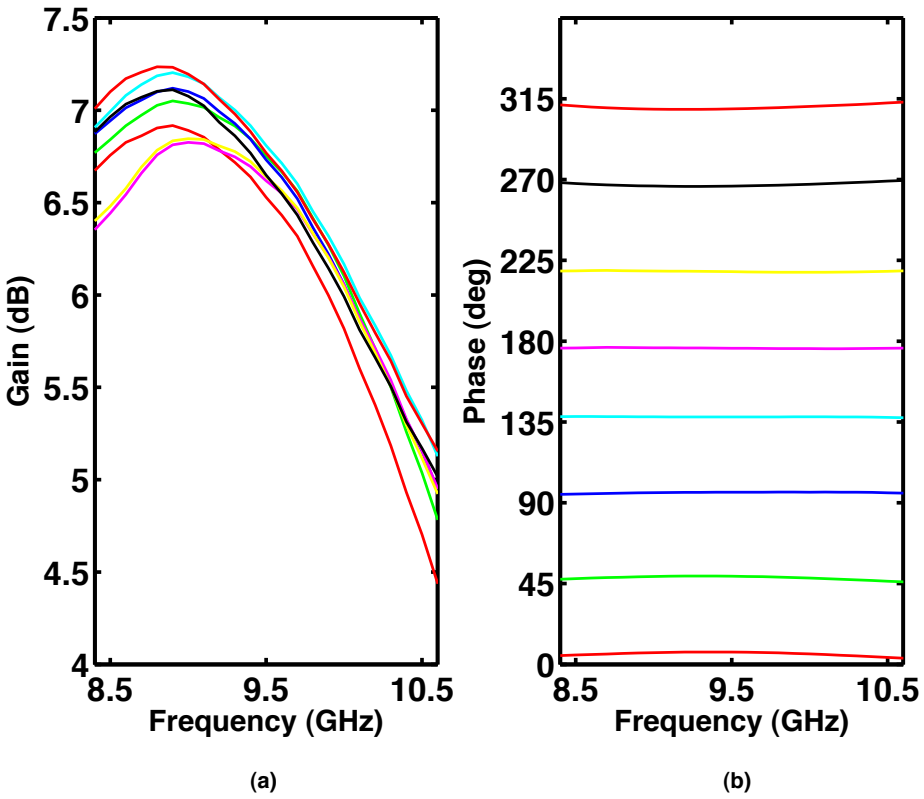


Figure 48: Gain (a) and phase (a) over all nine states for T/R module receiver. Maximum change in gain is 1 dB over 500 MHz bandwidth while phase spans full 0-360° in 45° increments.

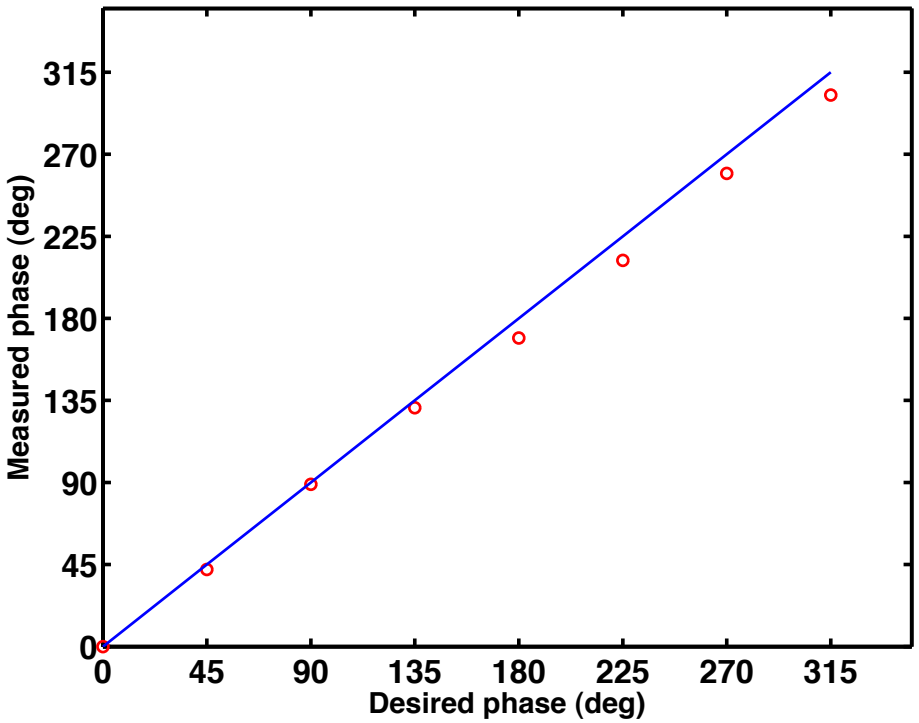


Figure 49: Measured versus desired phase at 9.5 GHz for all states of the SiGe T/R module receive path.

that the LNA is well noise matched. Lastly, noise circles for 9.5 GHz are plotted in Fig. 51, which show the minimum noise figure of 2.5 dB is very close to the center of the Smith chart, with the 2.6 dB noise circle encompassing 50 Ω. The T/R module is able to achieve very low noise figure due to optimizations with the LNA to provide low noise, with high gain, which reduces the impact of the lossy switches in the phase shifter.

Single and two-tone linearity was also characterized using two signal generators, a power meter, and a spectrum analyzer. For the one-tone measurement, a 9.5 GHz CW signal was swept from -27 to -5 dBm at the input of the T/R module. The input 1-dB compression point is determined to be -12.1 dBm with an output power of -6.78 dBm, as shown in Fig. 52, which plots the P_{out} vs. P_{in} in the solid blue line and the gain in the dashed red line.

The small-signal, two-tone linearity was also measured on the SiGe T/R module

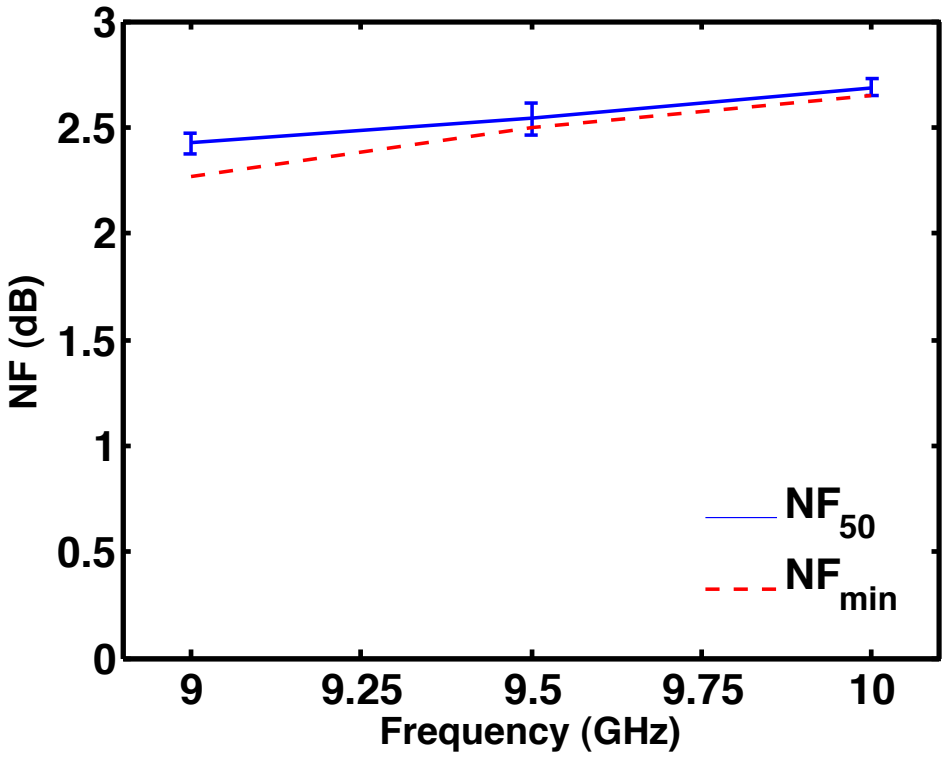


Figure 50: Minimum and 50 Ω noise figure across frequency of SiGe T/R module receive path in the 0° phase state.

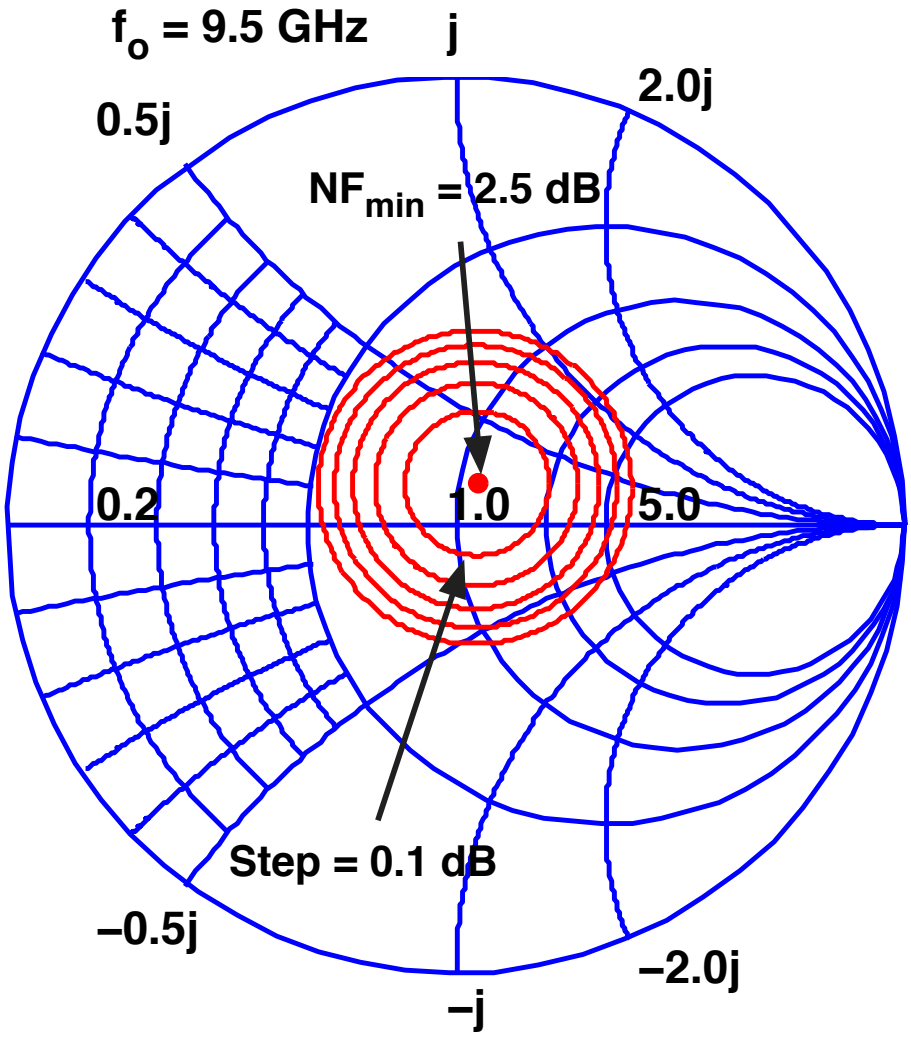


Figure 51: Noise circles at 9.5 GHz for SiGe T/R module in receive mode, showing a minimum noise figure of 2.5 dB with a good noise match to 50 Ω.

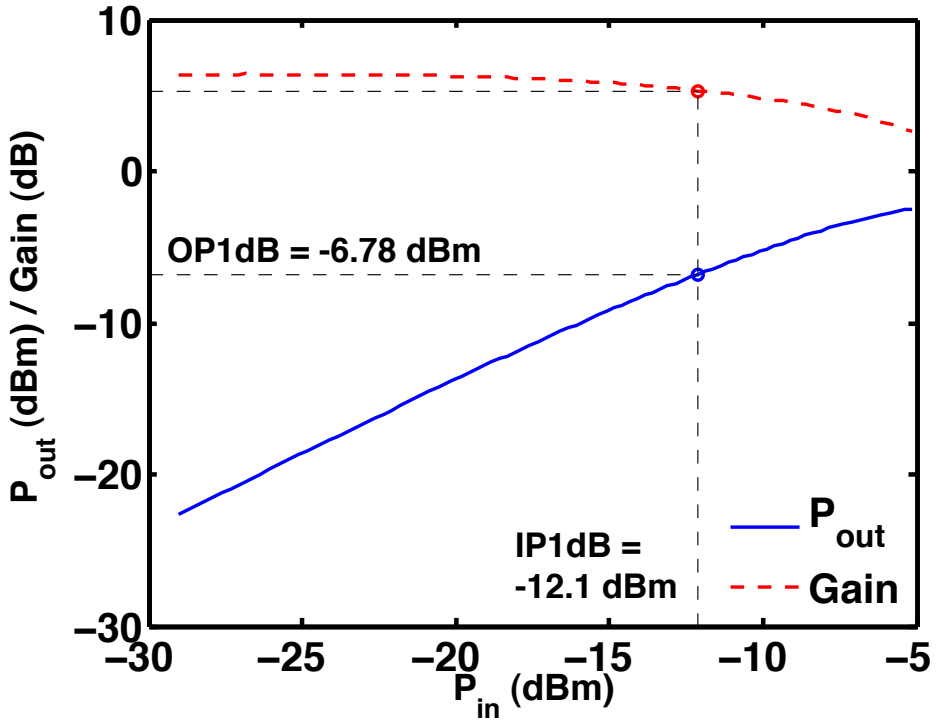


Figure 52: Ouput power and gain versus input power showing 1-dB compression point for SiGe T/R module receiver.

receiver. Input fundamental tones of 9.5 and 9.51 GHz were swept from -27 to -20 dBm of input power, yielding third-order intermodulation (IMD_3) tones of 9.49 and 9.52 GHz at the output. The fundamental and IMD_3 at 9.5 and 9.52 GHz (respectively) are plotted as function of input power, as shown in Fig. 53. The output third-order intercept (OIP_3) is determined to be 7.8 dBm. This figure of merit is calculated by finding the intersecting point of the extrapolated tones, which follows a 1:3 slope between the fundamental and IMD_3 tones.

A summary of the measured on-wafer performance is shown in Table 6, including a comparison with current state-of-the-art T/R modules. The 3-bit T/R module presented here demonstrates competitive performance to other SiGe and III-V T/R modules and maintains one of the lowest reported noise figures and highest linearity for a SiGe T/R module.

Table 6: Comparison of X-band T/R module performance.

Literature	Freq. Of Op.	Phase Res.	Gain	Noise Figure	IIP3	Power Diss.	Die Size	Technology
	GHz	Bits	dB	dB	dBm	mW	mm^2	
This work	8.5-10.5	3	7	2.5	0	35	9.25	200 GHz SiGe BiCMOS
[15]	8 - 10.7	5	11	4.1	-13	33	13.3	200 GHz SiGe BiCMOS
[86]	8 - 12	6	22	2.25	NR	NR	24.75	0.25 μm GaAs PHEMT
[28]	11 - 12	4	3.7	4.4	-17	53	1.5	80 GHz SiGe BiCMOS
[7]	8 - 12	7	10	< 9	> 11	NR	14.2	0.2 μm GaAs PHEMT
[36][1]	6 - 18	4	20	5	-18	561	5.39	150 GHz SiGe BiCMOS

NR = Not Reported. [1]for 8 channels

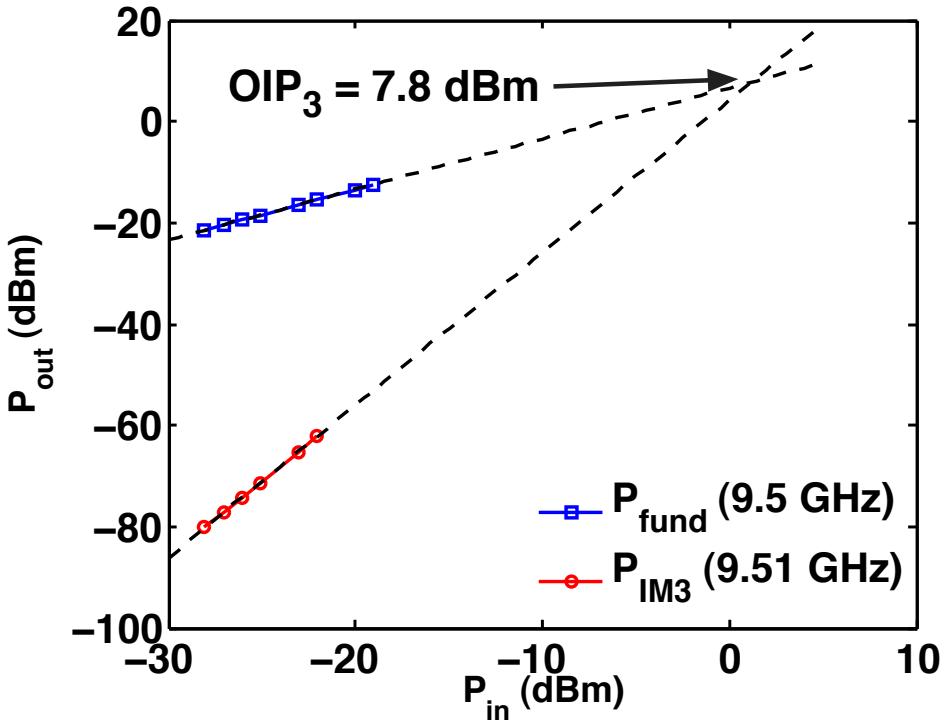
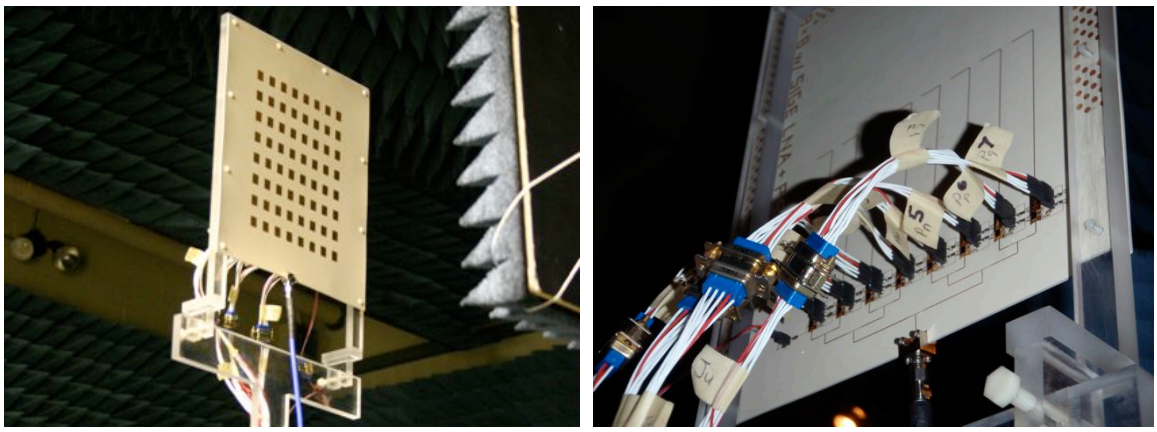


Figure 53: SiGe T/R module two-tone linearity at 9.5 GHz with 10 MHz tone spacing, yielding an output IP_3 of 7.8 dBm.



(a) (b)

Figure 54: Photograph of (a) frontside of the 8 x 8 element subarray and (b) back of subarray showing SiGe T/R modules in Georgia Tech Research Institute's near-field antenna range.

3.4 Antenna Results and Analysis

3.4.1 Measured Results

In order to verify operation of the array, a prototype 8 x 8 subarray was assembled and characterized in a near-field antenna range (NFR). The SiGe T/R modules are mounted and wirebonded to the array. Pin headers were soldered onto the array and interfaced to custom cables, which connect to the *dc* supply and FPGA I/O. Due to the flexible nature of LCP, the antenna array was mounted on a custom plexiglass frame as shown in Fig. 54 (a) that shows the subarray mounted in the anechoic chamber. Fig. 54 (b) is a photograph of the back of the array mounted in the chamber showing the SiGe T/R modules and cable assembly.

The NFR was used to measure the receive antenna patterns from 8.5 to 10.5 GHz for the subarray across the nine scan angles. An antenna probe (acting in transmit mode) rastered across the test antenna, while the received power is measured by a network analyzer. A cylindrical scan, where the antenna probe scans vertically while the array under test moves $\pm 180^\circ$, provides full side and back lobe characterization from $\pm 180^\circ$ in azimuth and $\pm 60^\circ$ in elevation. A total of nine scans of the array

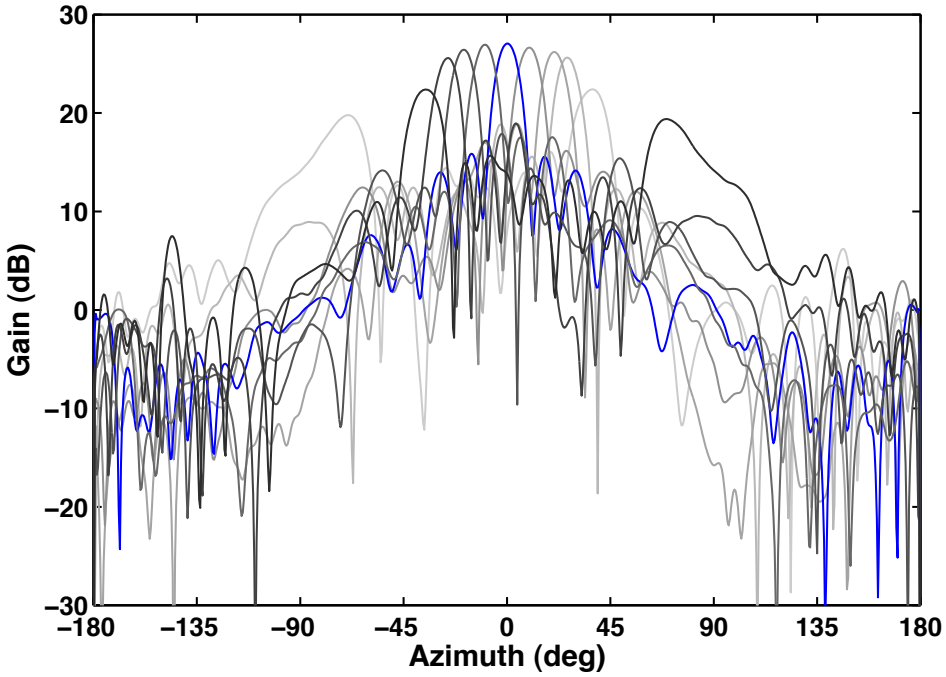


Figure 55: Measured antenna gain across azimuth at 9.5 GHz for 8 x 8 subarray for all 9 scan angles.

were performed, one for each desired scan angle. Automation software from Nearfield Systems, Inc. (NSI) was used to perform the measurements and calculate the far-field response.

The results from these measurements are shown in Fig. 55, which plots the antenna gain versus azimuth for all 9 scan angles at 9.5 GHz. The peak gain is over 27 dB which varies less than 1.5 dB as the array is scanned from ± 24.21°. The extreme scan angles of ±32.86° shows a reduction in gain and the appearance of grating lobes, which is expected given the array element spacing. The sidelobe levels are at least 10 dB lower than main beam, and can be improved with array tapering. The measured 3 dB beamwidths at broadside are 10.5° and 7° in the azimuth and elevation directions respectively. In addition, the direction of the peak gain the scanned beams were accurate to within 2° of the expected beam direction. Fig. 56 is a 2-D color surface plot of the antenna gain, highlighting low sidelobe levels and antenna beamwidths.

In order to verify the measured response with simulation, the normalized antenna

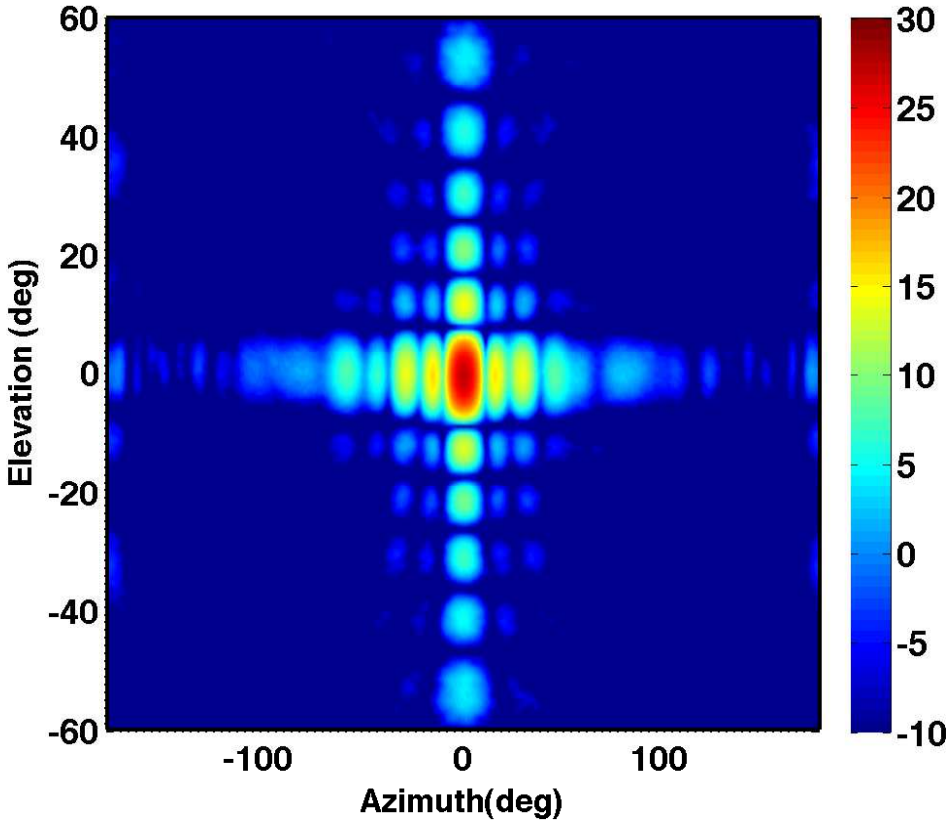


Figure 56: Color surface plot of antenna pattern of 8 x 8 subarray at 9.5 GHz highlighting low sidelobe levels, antenna gain, and beamwidth.

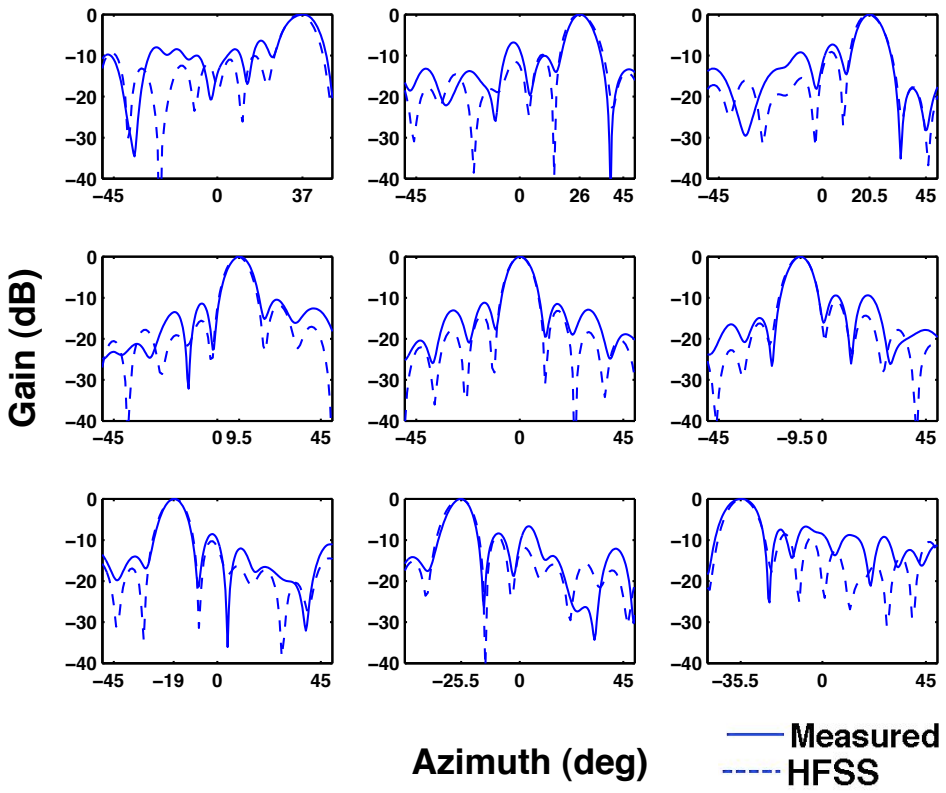


Figure 57: Measured versus HFSS simulated normalized antenna gains over azimuth at 9.5 GHz for all nine scan angles.

gain results for each of the 9 states are plotted in Fig. 57, which compares the measured gains with HFSS simulated results. The main beam and nulls match closely with simulation, with only slightly higher sidelobe levels. In addition, peak gain at broadside over frequency is plotted in Fig. 58. The antenna gain peaks near 9.5 GHz with a 2 dB bandwidth of over 1 GHz, which meets the requirements for the intended application.

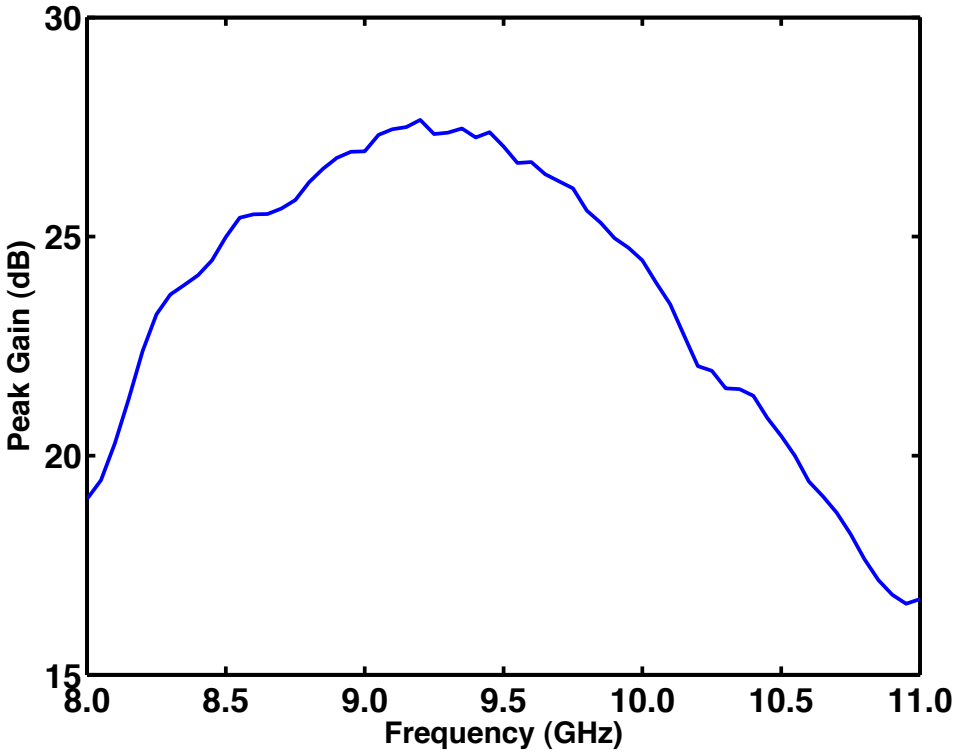


Figure 58: Measured peak antenna gain over frequency for broadside.

3.4.2 Receiver Noise Performance

In order to understand system impacts of using an active array, it is important to determine the added noise (due to losses and noise figure of the amplifiers) of the antenna on the system. One such metric is discussed in [37, 44], which introduces a figure-of-merit (FoM) ratio, antenna gain over effective system temperature, or G/T. This FoM is used to quantify the received noise performance of active array antenna and is a measure of signal-to-noise ratio of the system at the output. G/T is determined by calculating the total receive noise figure (including conductor and mismatch losses) and the directivity of the antenna.

In order to calculate G/T, the total noise figure of the receiver is calculated using Frii's equation for cascaded noise figure in Eqn. 12. For the SiGe T/R chips, the noise figure (F_{TR}) and gain (G_{TR}) was measured to be 2.5 dB and 7 dB, respectively, as shown in Section 3.3.5. For the radiating elements and feed networks, HFSS was used to simulate the conductor and mismatch losses. The loss before the TR chip (L_{ant}) is 3.9 dB and mismatch loss (L_{R1}) is simulated to be 0.1 dB. The losses after the SiGe TR chip (L_p) should be similar to the power divider losses before the SiGe chip, and are taken to be 3.9 dB. From this equation, it is clear that when the T/R gain is sufficiently large, the feed line loss and T/R noise figure will have the most effect on performance and the components following the chip will have a negligible effect.

$$F_T = L_{ant} + (F_{TR} - 1)L_{ant}L_{R1} + \frac{L_p}{G_{TR}} \tag{12}$$

$$\frac{G}{T} = \frac{D}{T_o(F_T - 1)} \tag{13}$$

The directivity for the 8x8 subarray was determined to be 20 dBi using the measured radiation patterns at 9.5 GHz. The NF of the antenna array is 7.1 dB, thus

using Equ 13, the G/T is calculated to be -10.8 dB/K. In the full 2304 element array, the directivity will be higher, and the estimated G/T would be above 10 dB/K. For this antenna, the ohmic feed line loss, L_{ant}, has the largest impact on the G/T ratio. In order to improve this FoM, SiGe T/R chips can be added closer to the radiating elements, thereby reducing the impact of the feed losses, decreasing receiver noise figure, and increasing G/T.

3.5 Summary

This research represents the first demonstration of an X-band integrated 64 element active phased array receiver using SiGe and organic multilayer (LCP+Duroid) technologies. The design and measurement of the antenna, SiGe T/R module, and integrated subarray antenna is presented. In addition, the design of the FPGA digital control board is also presented, which enables beamsteering and control of the phase shifters. This receive subarray is designed for use in snow and cold land processing applications and meets performance, cost, and size requirements for use with compact platforms, such as UAVs.

The SiGe T/R module receiver was characterized on wafer using an integrated S-parameter, load-pull, and noise test setup. The receiver gain was over 7 dB, with a noise figure of less than 2.5 dB at 9.5 GHz. The OIP_3 was measured to be 7.8 dBm and output 1-dB compression is greater than -7 dBm. The receiver dissipates 35 mW of *dc* power during operation, and only 3.5 mW in standby.

Lastly, the SiGe T/R module was integrated onto a multilayer antenna to demonstrate the 8 x 8 receive antenna. The antenna was characterized in a NFR facility, and nine total scan angles were measured. A FPGA was programmed to allow simple beamsteering through a computer interface. The antenna patterns demonstrate correct beamsteering with a peak broadside gain of over 27 dB with sidelobes less than -10 dB. The G/T for the subarray was calculated to be -10.8 dB/K and is estimated

to be above 10 dB/K for the full array.

In summary, this research demonstrates the ability for the integration of advanced technologies, such as SiGe and LCP, to meet the needs of advanced active phased array antenna systems. These technologies provide lower cost, light weight, highly integrated, and compact solutions while still meeting the required performance for these systems. In the following chapter, circuit blocks used in this T/R module will be characterized at low-temperature to determine the effects of using these modules across wide-temperature ranges.

CHAPTER IV

CHARACTERIZATION OF RF AMPLIFIERS FOR LOW-TEMPERATURE OPERATION

4.1 Introduction

The RF performance of SiGe HBTs have been shown to greatly improved by cooling [82,92]. In this chapter, I explore the performance of SiGe HBT based-LNAs across wide-temperature operation. The first results highlight the gain and noise figure of packaged LNAs that were characterized at 15 K physical temperature. In addition to this measurement, new novel on-wafer characterization techniques allowing measurement of S-parameters, noise figure, and linearity is presented, which can aid in fully understand impacts of low-temperature operation on LNA performance. On-wafer testing of these parameters greatly facilitate both circuit and device characterization.

Many emerging applications for extreme environments require amplifiers operating in wide-temperature ranges traditionally outside of military specifications (-55 C to +125C), where foundry provided design kit models are untested. Therefore, characterizing both circuit and device performance over an extended temperature range is necessary. SiGe HBT have been shown to large improvements through cooling, approaching half-terahertz performance at deep-cryogenic temperatures [92], which will likely result in a large increase in other RF parameters.

In this research, a SiGe HBT LNA is measured over the range from 173 K - 300 K. RF characteristics such as S-parameters, noise figure, and linearity of the LNA and devices are measured across these temperatures. In addition, an npn SiGe HBT device noise characteristics are measured from 150 K - 300 K. The major challenge of this effort is achieving accurate noise figure and linearity calibrations to ensure high

quality measurements. Measuring these parameters over a wide-temperature range proves to be difficult due to the complexities of the measurement system and ensuring accurate calibration. For both measurements, especially noise figure, characterizing losses are critical to ensuring accurate results, as any error would directly effect the measurement of the RF parameters. A novel technique to correctly calibrate losses will be used in order to ensure the validity of the measurements.

In the previous chapters, we examined high-frequency LNAs for use in radar and communication systems. Another important application for LNAs is in radio astronomy receivers. These receivers require a very high level of sensitivity due to the extremely low signal levels of cosmic radiation. The amplifiers are typically cryogenically cooled to help improve noise performance. Currently, most of these cryogenic amplifiers use InP HEMT or other III-V technology [5,66,90]. The potential for SiGe HBTs in cryogenic environments has been shown in [4,38,93]. These articles allude to the possible performance improvements using SiGe HBTs in cryogenic high-frequency circuits such as LNAs.

In section 4.2, I examine some of the low-temperature *dc* and *ac* performance improvements of SiGe HBTs. Section 4.3 introduce the cryogenic noise measurement technique and review the challenges of measuring very low noise figure devices. Section 4.3.2 we will highlight the results of two SiGe HBT LNAs operating at 15 K physical temperature. Sections 4.4 and 4.5 present on-wafer noise figure and linearity measurement setups and results (respectively). Section 4.6 concludes this chapter with a summary.

4.2 SiGe HBT Cryogenic Performance

As mentioned in section 1.1.1, the performance enhancements of SiGe HBTs are thermally activated, therefore, as these devices are operated in cryogenic environments, their performance greatly increases. Reviewing Equation (1) show that two terms:

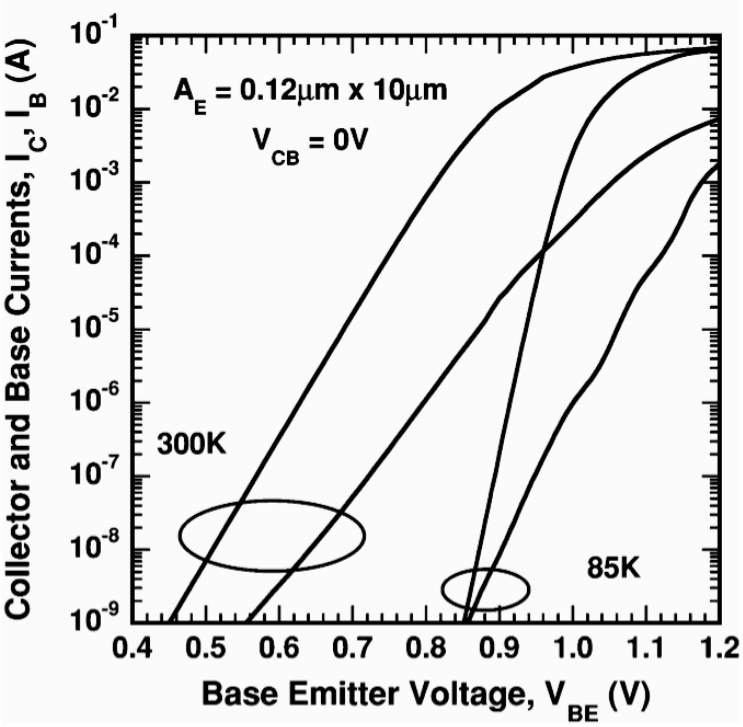


Figure 59: Forward Gummel characteristics for third-generation 0.12 × x 10.0 μm^2 SiGe HBT at 300K and 85K [4].

$\Delta E_{g,Ge}(grade)/kT$ and $\Delta E_{g,Ge}(0)/kT$ are aligned such that a decrease in temperature increases the current gain (β), which improves the *dc* and *ac* performance of the device. Figure 59 depicts the Gummel characteristics of a third-generation SiGe HBT at both 300K and 85K [4]. Figure 60 highlights the improvement in *dc* performance as the peak β increases from 500 at 300K to almost 4000 at 85K. Lastly, improvements in SiGe HBT *ac* performance can be evidenced in Figure 61, which plots f_t as function of collector current at 300K and 85K. This plots shows a greater than 50 GHz improvement in peak f_t which is expected as the drift field is increased in the base [21]. Thus, the bandgap engineering pursued to improve room temperature performance, also aims to improve low temperature performance of SiGe HBTs. These performance improvements will also enhance device noise parameters as these relations heavily rely on β and f_t, therefore, we can expect improvements in amplifier noise performance as these devices are cooled.

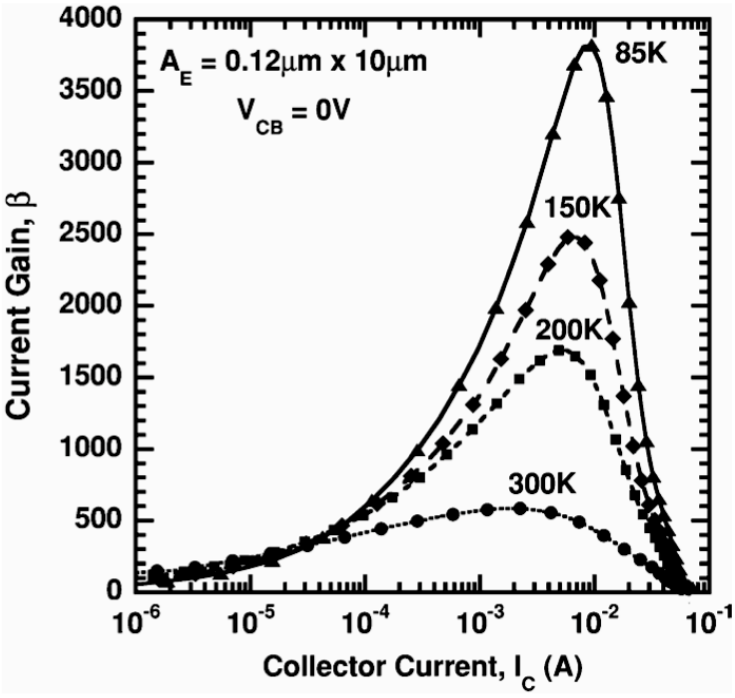


Figure 60: *dc* current gain, β, as a function of collector current for third-generation 0.12 $\times$ x 10.0 μm^2 SiGe HBT at 300K and 85K [4].

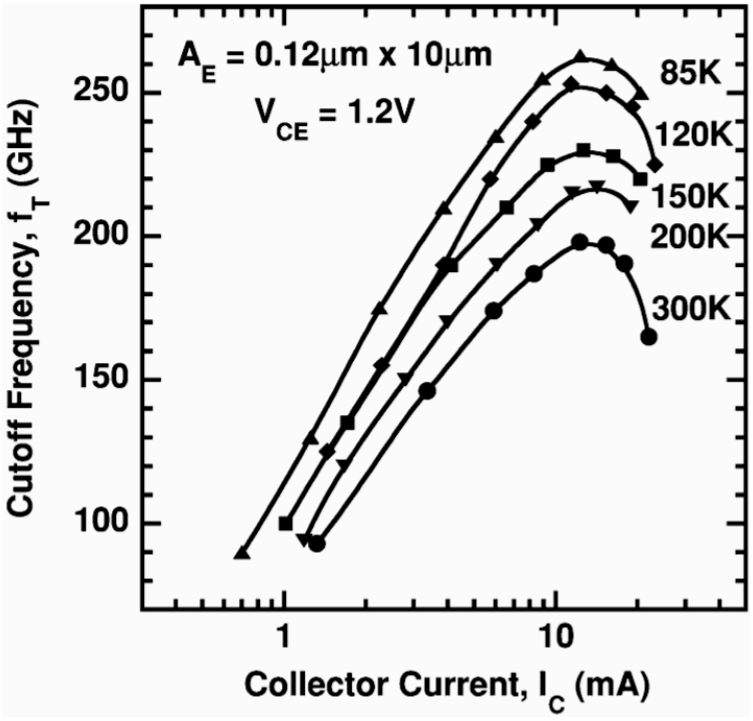


Figure 61: Cutoff frequency (f_t) as a function of collector current for a third-generation 0.12 $\times$ x 10.0 μm^2 SiGe HBT [4].

4.3 Cryogenic Noise Measurement of packaged SiGe HBT LNAs

4.3.1 Noise Measurement Technique

A serious challenge in designing cryogenic LNAs is the ability to accurately measure extremely low noise figures. The cryogenic measurement of the packaged LNAs were performed using the cold attenuator method and conducted at the CalTech RF and Microwave Group Facility in Pasadena California [89].

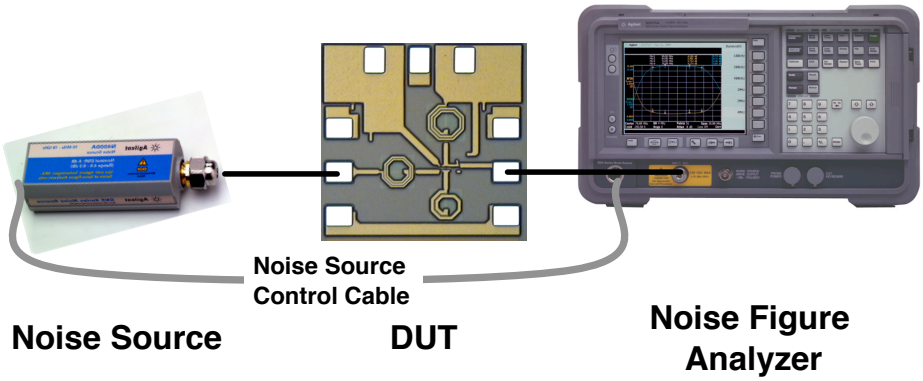


Figure 62: Noise measurement setup using the Y-factor method.

As shown in Figure 62, the Y-factor noise measurement requires a noise source and a noise figure analyzer (NFA). The purpose of the noise source is to provide a calibrated input noise power, typically referred to as an Excess Noise Ratio (ENR). The ENR is quoted in dB and varies over frequency for a given noise source:

$$ENR_{dB} = 10 \log \frac{T_s^{ON} - T_s^{OFF}}{T_o} \tag{14}$$

where T_s^{ON} and T_s^{OFF} are the noise temperatures of the noise source in its off and on state respectively, and T_o is the reference temperature of 290 K. T_s^{OFF} is calibrated to this reference temperature. For a given noise source, the ENR values will be specified over frequency and are specific to that noise source. These values are directly entered into the NFA and used for calibration and measurement. The Y-factor, shown in Equation (15), is the ratio of two noise power levels or noise temperatures. This ratio

depends on the ENR of the noise source.

$$Y_2 = \frac{N_2}{N_1} = \frac{T^{ON}}{T^{OFF}} \tag{15}$$

where N_2, N_1 is the noise power recorded when the noise source is on, off respectively. In order to calibrate the output losses, the noise source is connected directly to the output cable of the DUT. Since the ENR table is known, the NFA is able to determine the appropriate correction factors and calibrate any losses. If the noise of the instrument and output cables is T_2, the the Y-factor can be computed as:

$$Y = \frac{T_s^{ON} + T_2}{T_s^{OFF} + T_2} \tag{16}$$

solving for T_2 yields:

$$T_2 = \frac{T_s^{ON} - Y_2 T_s^{OFF}}{Y_2 - 1} \tag{17}$$

Once this measurement has been completed, the NFA normalizes its noise figure and gain calibration by applying the appropriate correction factor for T_2 and the DUT can be connected as shown in Figure 62. A similar measurement is made with the DUT in place, and the noise of both the DUT and the output cables and instrumentation is measured as T_{12}:

$$T_{12} = \frac{T_s^{ON} - Y_{12} T_s^{OFF}}{Y_{12} - 1} \tag{18}$$

where Y_{12} is the ratio of the noise powers of both the DUT and measurement equipment as measured between the ON and OFF states. Since T_2 is known, the noise of the DUT can be calculated:

$$T_{DUT} = T_{12} - \frac{T_2}{G_a} \tag{19}$$

where G_a is the gain of the DUT computed by taking the ratio of the noise power differences. Figure 63 is an illustration of how the Y-factor method can also be understood graphically [2]. In this graph, the output power from the DUT is plotted against the source temperature and since the DUT has a linear noise response, the

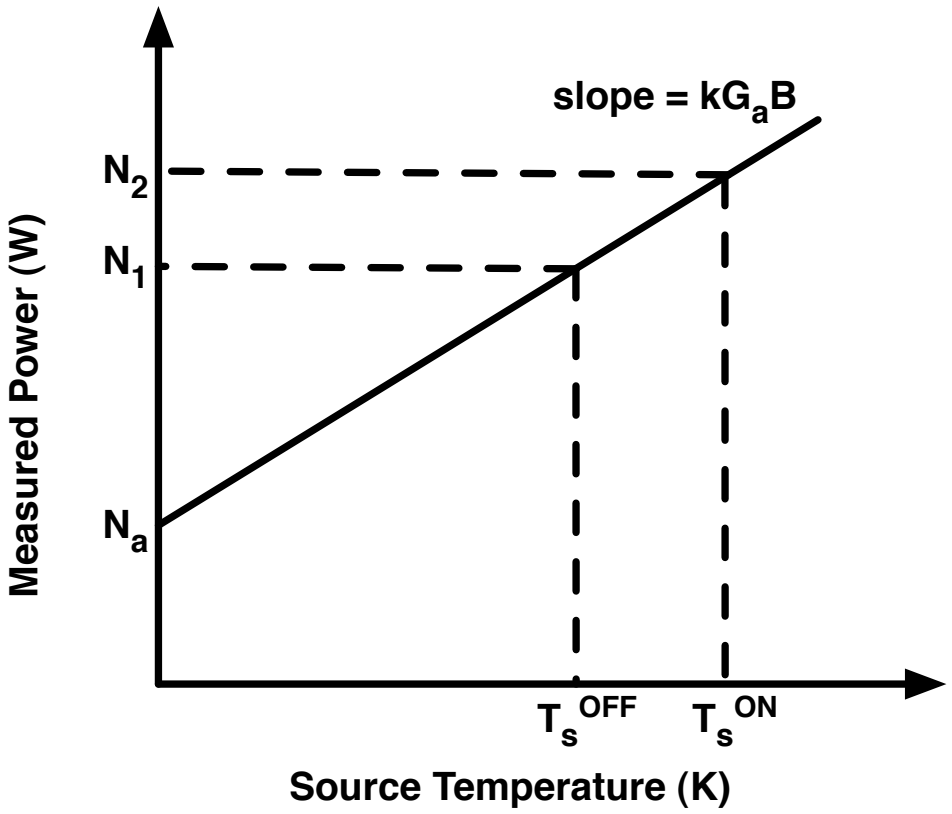


Figure 63: Noise power output versus source temperature for determining DUT noise power.

slope of this line is kG$_a$B where k is Boltzmann's constant and B is the measurement noise bandwidth.

By measuring two points on the line (T_s^{ON}, N_2) and (T_s^{OFF}, N_1), the slope and the y-intercept, N_a, can be determined through simple algebra. Solving for N_a, which is the added noise power by the DUT, yields:

$$N_a = N_1 - \left(\frac{N_2 - N_1}{T_s^{ON} - T_s^{OFF}}\right) T_s^{OFF} \tag{20}$$

Combining this relationship with the Equations (14) and (15) and taking $T_s^{OFF} = T_o$, the added noise power of the DUT in terms of the source ENR and the Y-factor is $N_a = kT_oBG\left(\frac{ENR}{Y-1} - 1\right)$

The Y-factor method is a straight-forward and accurate approach to measuring

amplifier noise performance. However, two of the primary sources of error for measuring noise figure across at these temperatures are accurately calibrating the losses between the noise source and the DUT and determining the temperature of these losses, since the physical temperature is not T_o. In addition, impedance mismatches, uncertainty of the noise source excess-noise ratio (ENR), and temperature fluctuations could also contribute to uncertainty and limit the accuracy of this measurement.

For very low noise applications such as radio astronomy receivers, effective noise temperature, T_e, is a more common metric used to define amplifier noise performance. T_e is the equivalent temperature of a resistor ($v_t^2 = 4kTBR\Delta f$) that would produce the same added noise at the output of a noiseless DUT. It is typically defined as:

$$T_e = \frac{N_a}{kGB}. \tag{21}$$

Noise temperature can be related to noise factor by the following relation:

$$T_e = T_o(F - 1). \tag{22}$$

Noise temperature is used in these applications since the input noise level from looking into space is much less than 290 K, therefore, the relationship between noise figure and SNR degradation cannot be directly calculated. This effect is due to the fact that noise figure is defined for a source impedance temperature of 290 K and SNR degradation is function of the source temperature [2]. Therefore the relationship, $SNR_{out} = SNR_{in} + NF$ is not valid if temperature of the source impedances are different. For these reasons, the noise performance given for the amplifiers in the remainder of this section will be in terms of T_e.

For a room temperature noise measurement, the off state for the diode noise source is approximately 300 K. The ENR of the noise sources have a finite error ($\pm$ 1 %), which yields a variation of noise temperature of approximately 10 K [1]. This uncertainty limits the minimum resolution to between 0.1 - 0.2 dB. In addition to this source of error, there is typically an impedance difference between the off

and on states of the noise source which also increases the measurement uncertainty. These uncertainties prevent the characterization of very low noise temperatures, and therefore the standard noise measurement method will not yield reliable results in a cryogenic environment.

The cold attenuator method overcomes these uncertainties by inserting a temperature calibrated 20 dB pad at the input of amplifier. This attenuator lowers the effective temperature as presented to the DUT of the noise source and reduces the measurement uncertainty by a factor of 100. When the noise source is in the off state, the noise presented to the amplifier is the physical temperature of the cryogenic pad, 15 K, plus a contribution from the diode noise source which is attenuated by 20 dB yielding a total noise temperature of 18 K. When the noise source is on, noise temperature at the output of the noise source is approximately 9000 K which is reduced by the attenuator to 90 K, including the attenuator noise, the total noise temperature is 105 K. Therefore, the off and on noise temperatures presented to the amplifiers is reduced to 18 K and 105 K respectively, in addition, any errors due to the uncertainties of the noise source are also reduced, thus enabling accurate measurement of cryogenic amplifiers with noise temperatures below 50K [23].

In order to de-embed the noise figure of the amplifier, the temperature of the attenuator and any cables must be known very accurately. A calibrated temperature sensor is affixed to the attenuator and a system verification was performed to determine the correction factor to enter into the Agilent N8975A Noise Figure Analyzer (NFA). The analyzer has the ability to de-embed losses at a different temperature both before and after the DUT and calculates the corrected noise temperature using the standard Y-factor noise measurement method discussed earlier. The measurement setup is shown in Figure 64, with the expanded view highlighting the internal dewar connections and the cold attenuator with the temperature sensor.

The measurement facility discussed here has been extensively used to measure

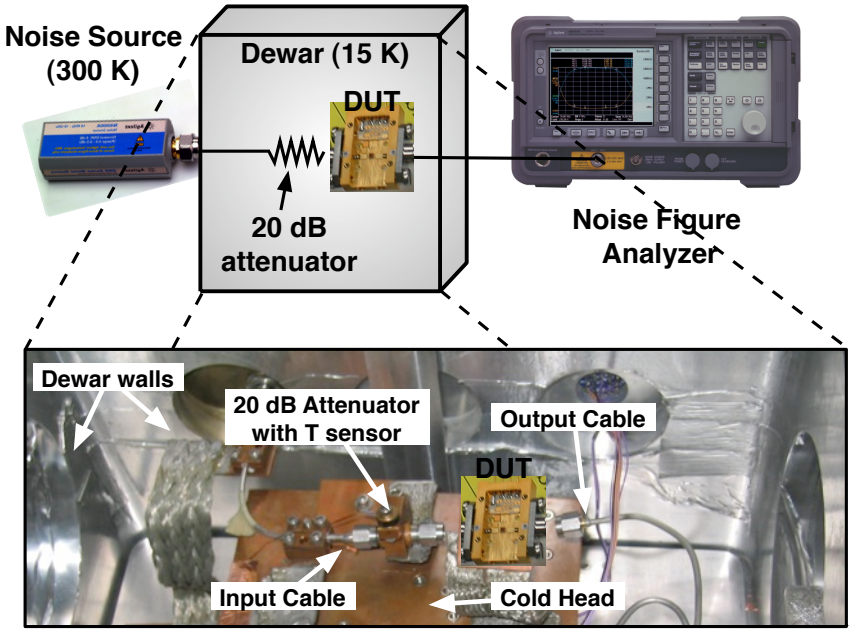


Figure 64: Schematic of cryogenic measurement setup with expanded view of inside dewar.

noise figures of a variety of cryogenic amplifiers. The system has been verified against a National Institute of Standards and Technology (NIST) characterized cryogenic amplifier [23]. The remaining section discusses the results from measuring SiGe HBTs X-band LNAs in this cryogenic noise measurement setup.

4.3.2 Results from Cryogenic Measurement of SiGe HBT LNAs

The inductively-degenerated cascode LNA (referred to as LNA - A) [41] and the modified low-power variant (referred to as LNA - B) [74] were measured using the cryogenic noise measurement system discussed in the previous section. Neither LNA was specifically designed for low temperature operation, however, the bias currents were adjusted appropriately to achieve the lowest noise temperature performance. Figure 65 shows an example of LNA - A mounted in the package for cryogenic testing.

Both LNAs were cooled to 15 K and noise and gain performance were measured. Figure 66 and 67 shows the cryogenic performance of LNA-A / LNA-B respectively. The room temperature performance of LNA - A in fixture varies only slightly from

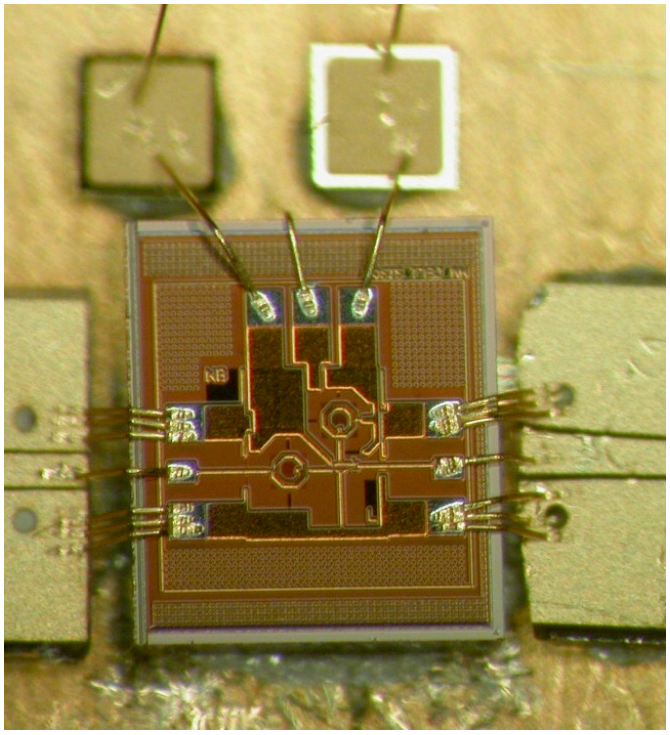


Figure 65: Photograph of X-band LNA in package for cryogenic testing.

the corresponding on-wafer measurements. These room temperature measurement shows a gain of above 17 dB across band and a noise performance of above 170 K (2 dB noise figure) while dissipating 15 mW of *dc* power. As shown in Figure 66, LNA-A's cyrogenic noise performance is improved dramatically with T_e below 21K (0.3 dB noise figure) and dissipating only 2.25 mW of *dc* power. The approximate 1-2 dB reduction in gain is due to the change in collector current (approximately 5 mA) which was selected to minimize noise.

Similar performance improvements can be shown for LNA-B operating at a physical temperature of 15 K. Figure 67 shows over a 150 K reduction in T_e and an almost 5 dB increase in gain across the band. Since LNA - B was optimized for lower current, the operating points between the room and low temperature measurement were similar with only 0.2 mA change in collector current therefore there is a gain enhancement in contrast to the gain degradation from the LNA - A measurement.

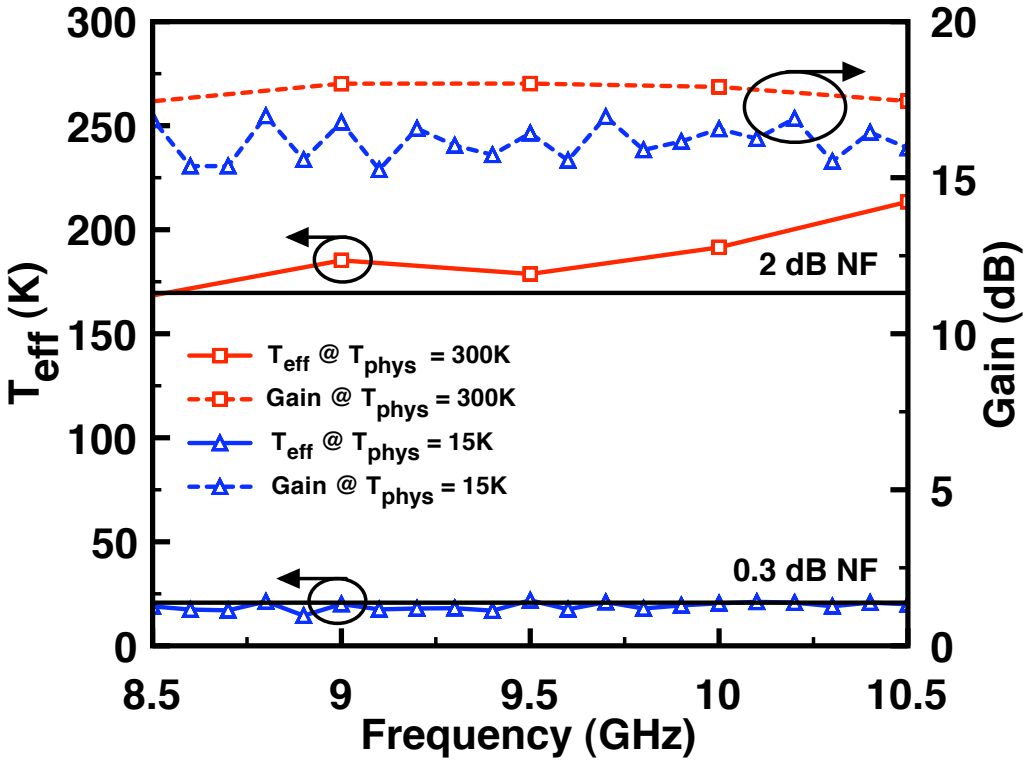


Figure 66: Effective noise temperature (K) and gain (dB) of the X-band LNA - A at 300K and 15K.

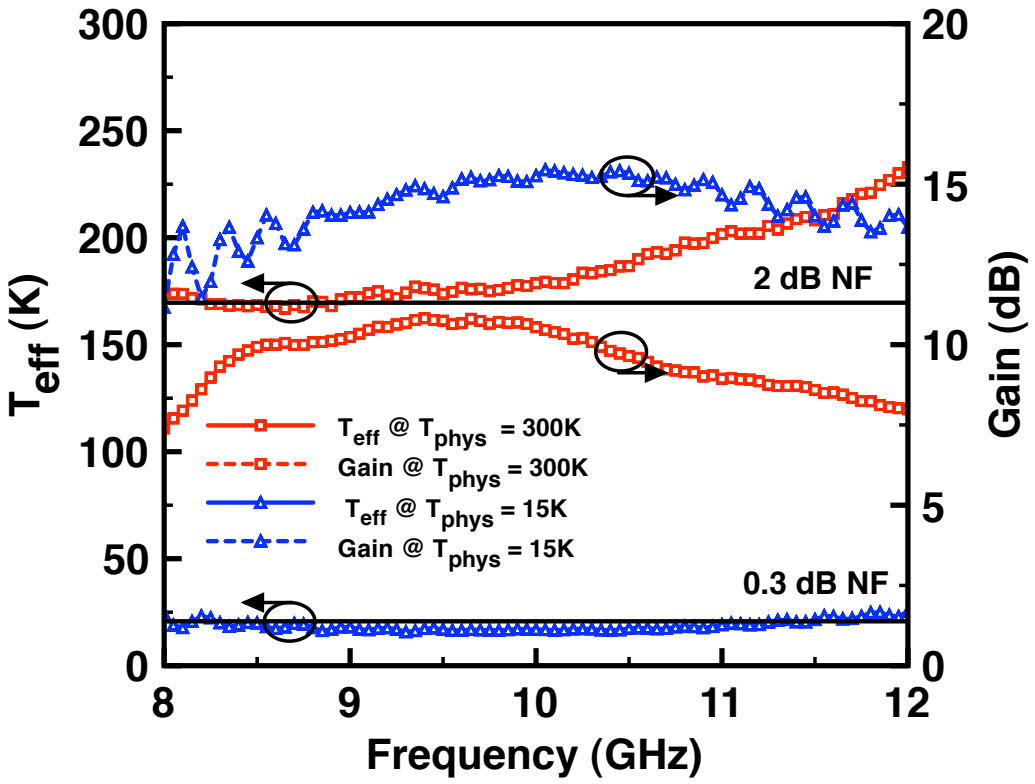


Figure 67: Effective noise temperature (K) and gain (dB) of the X-band LNA - B at 300K and 15K.

4.4 On-Wafer Low-Temperature Noise Figure Characterization

4.4.1 Measurement Setup and Methodology

In the previous section, the cold-attenutor method was used to characterize noise figures of LNAs at deep-cryogenic temperatures. However, this technique is not compatible with on-wafer characterization, and requires a dedicated, pre-calibrated noise measurement dewar. An alternate technique to characterize noise figures to moderately low temperatures (verified to 150 K) is presented in this section. This technique is able to accurately account for input/output losses and calibrate the results to a passive resistor structure, correcting for any errors introduced by the temperature gradient of the feedlines.

The low-temperature measurement setup is shown in Fig. 68 and uses the Y-factor (also referred to as the hot/cold) method to determine the noise figure of the DUT. The setup consists of a network analyzer, two RF switches, noise figure analyzer, noise source, LNA, isolator, and an on-wafer cryogenic dewar chamber.

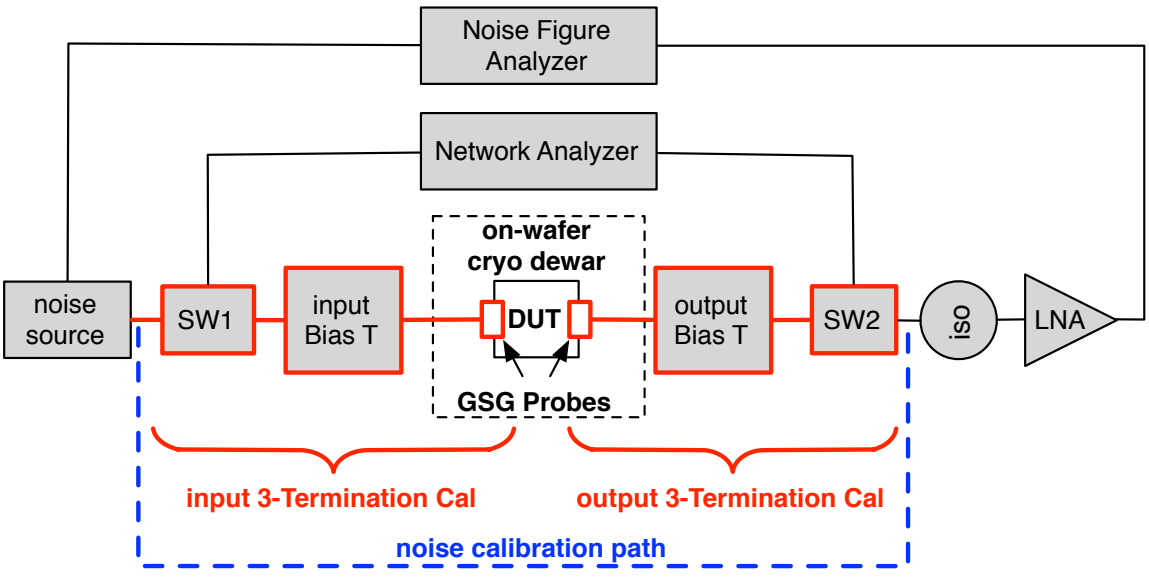


Figure 68: Technique for noise figure measurement at low-temperatures using the "3T" calibration method of determining input and output losses.

In order to account for the losses between the noise source and DUT, a calibration technique call "3 termination" (or 3T) calibration can be performed. In this procedure, the two-port S-parameters of a reciprocal passive network, which cannot be directly measured, such as inside the on-wafer cryo dewar, are able to extracted by measuring three one-port measurements.

Once this calibration is performed, both the input and output loss from these S-parameters can be entered into the NFA, where the NFA can be calibrated to the cable level with the path shown in Fig. 68. The next step in the calibration procedure is to correct for the temperature variation of the losses from the feedline and probes in the cryogenic dewar. At room temperature, the losses would directly correspond to noise figure, however, since this is not the case, a temperature correction must be applied. Since the feedline and probes experience a temperature gradient, going from 300K at the input/output port, to measurement temperature at the probe tips, a simple temperature reading will not suffice.

In order to correct for this effect, measurement of a passive resistive divider test structure can be used to empirically correct for this deviation. From the S-parameters of this test structure, the noise parameters can be calculated from the following equations:

$$G_{21} = \frac{|S_{21}|^2(1-|\Gamma_s|^2)}{|1-S_{11}\Gamma_s|^2(1-|\Gamma_{out}|^2)} \tag{23}$$

where G_{21} is the associated gain, Γ_s is the source reflection coefficient (taken to be 50 Ω), and Γ_{out} is the output reflection coefficient, which is determined from the s-parameters of the DUT; and:

$$F_{s2p} = \frac{1+(T_2 - G_{21}T_1)}{G_{21}T_o} \tag{24}$$

where T_o is the standard temperature of 290 K, T_1 is the temperature of the measurement setup, and T_2 is the temperature of the DUT.

Once the noise figure is extracted from the S-parameters, these results can be

compared against the results from the noise figure measurement method. An offset in the temperature of the losses can be entered into the NFA, which can be used to correct for any deviations in the noise parameters extracted from the S-parameters and the noise measurement method, helping correct for this temperature gradient.

4.4.2 SiGe HBT LNA and *npn* Device Results

Using the calibration and measurement technique described above, an X-band low-power LNA was characterized at 193, 218, and 300 K. In addition, this LNA was measured at different *dc* power conditions of 0.5, 1, and 2 mW of power dissipation. Details on the LNA design can be found in [74]. At room temperature, the LNA was measured to have 10 dB of gain, and less than 2 dB noise figure.

Fig. 69 highlights the noise from 8 - 12 GHz with 2 mW of power dissipation, at the three temperature points. It is clearly noted that there is a large decrease in noise across the entire band from room temperature to 193 K. However, while there is a 0.75 dB decrease in noise figure from 300 to 213 K, there is only a 0.1 dB decrease from 213 K to 193 K. Similar trends are observed in the gain measurements are observed in Fig. 70, with a large improvement in gain (over 2 dB) from 300 to 213 K, but only a slight improvement from 213 to 193 K (less than 1 dB).

By plotting the mean noise figure as a function of temperature, a clear trend of decreasing noise figure can be seen in Fig. 71, which is expected given the large improvement of RF performance for SiGe HBTs at low temperatures. By examining the slope, it appears that a 100 K change in temperature, reduced the noise figure by approximately 50 %. These results appear to be consistent with the noise figure reported in [82], which reports less than 0.3 dB noise figure at 15 K.

Observing the average noise figure as a function of dissipated power (achieved by changing the collector current), there is a large increase in noise figure below 1 mW of power dissipation as shown in Fig. 72. However, only a small change in noise figure

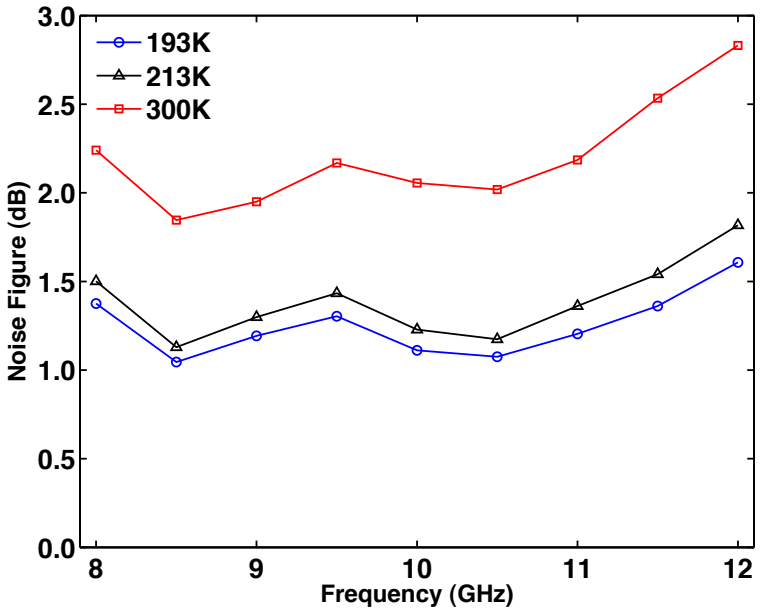


Figure 69: Noise figure at 300, 218, and 193 K for the low-power X-band LNA measured using the proposed on-wafer cryogenic noise measurement setup.

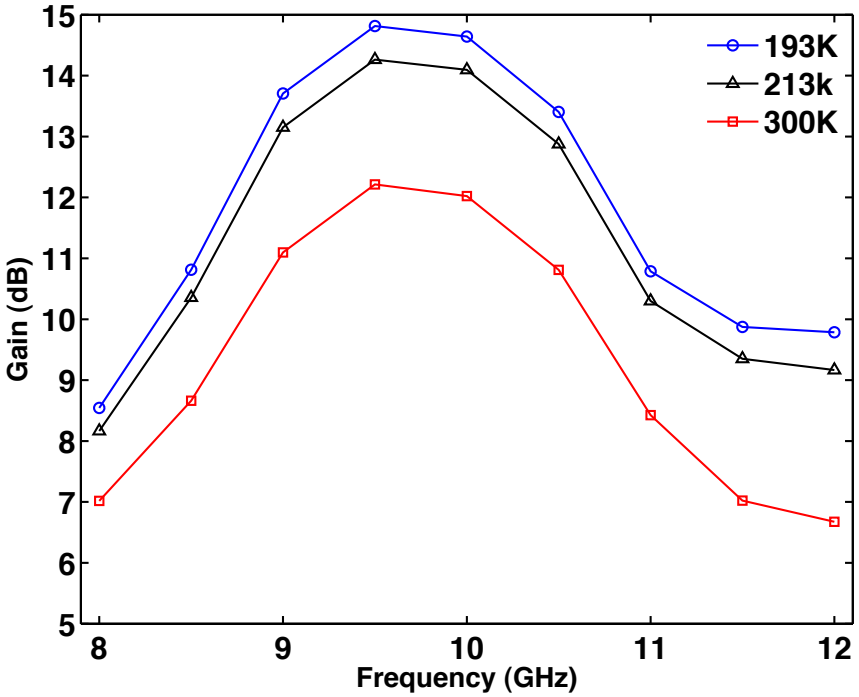


Figure 70: Gain at 300, 218, and 193 K for the low-power X-band LNA.

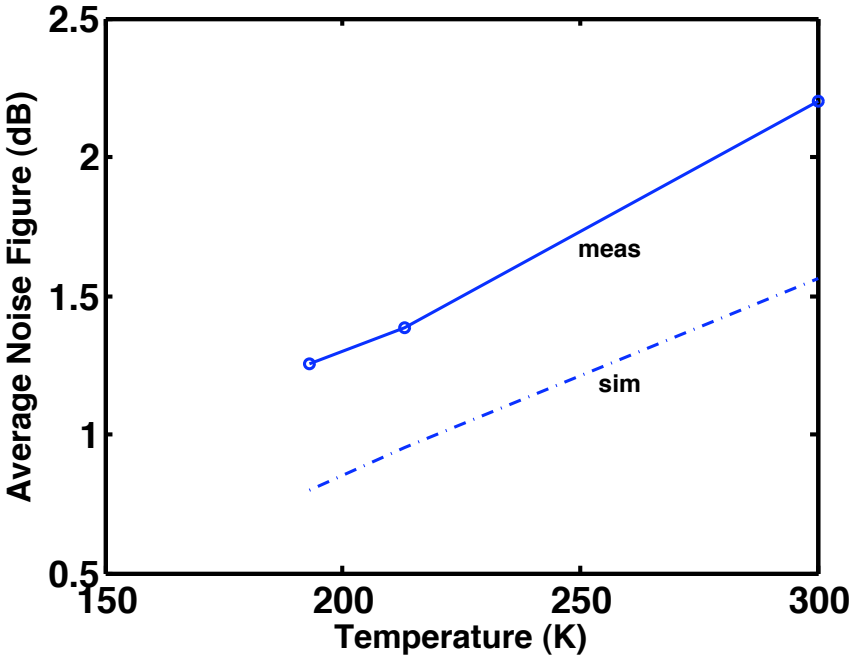


Figure 71: Mean noise figure as function of temperature for the low-power X-band LNA at 2 mW *dc* power dissipation as compared to simulated results.

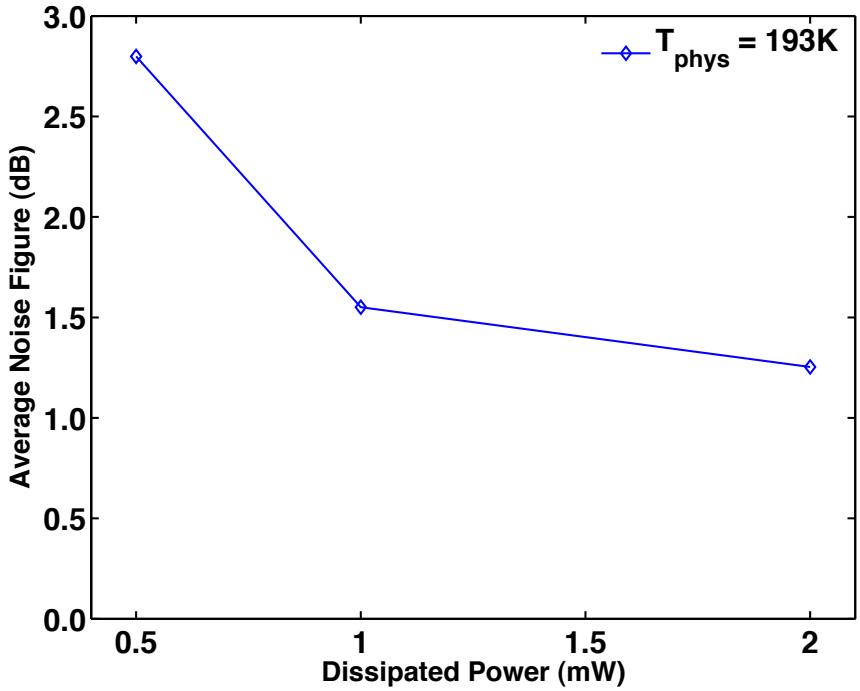


Figure 72: Mean noise figure as a function of dissipated *dc* power for the low-power X-band LNA at 193 K.

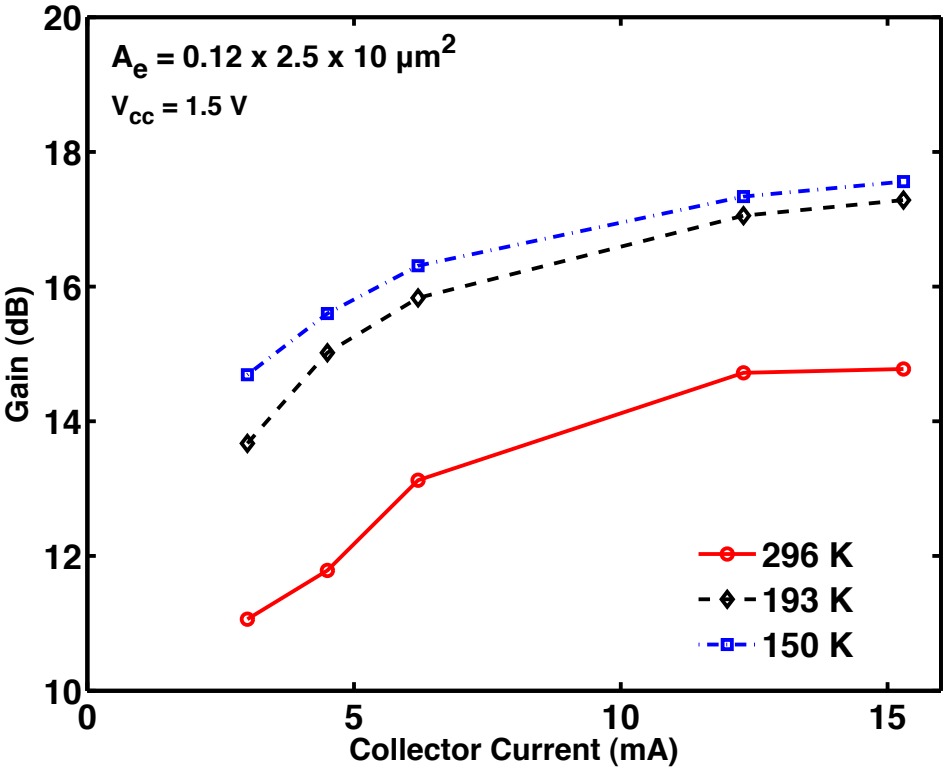


Figure 73: Gain of SiGe HBT npn (A_E = 0.12 x 2.5 x 10 μm^2) at 9.5 GHz as a function of collector current for 296, 193, and 150 K.

is observed by reducing the power from 2 to 1 mW.

In addition to characterizing an amplifier circuit, SiGe HBT devices can also be measured using the proposed on-wafer cryogenic noise measurement setup. For these measurements, a third generation npn SiGe HBT with an emitter area of 0.12 x 2.5 x 10 μm^2 was characterized from 296 to 150 K at different collector currents. The device was measured using a standard test structure, and results include the bondpads and metal transitions to the device, and is not de-embedded to remove their effects. The npn is biased to a V_{cc} of 1.5 V with currents ranging from 3 - 15 mA or current densities from 1 - 5 mA/μm^2 that cover regions both below and near peak f_T.

Fig. 73 plots the gain at 9.5 GHz as a function of collector current. The gain exhibits typical performance improvements, highlighting increase in gain for both low temperature and higher currents. In addition, a large boost in gain occurs from 296

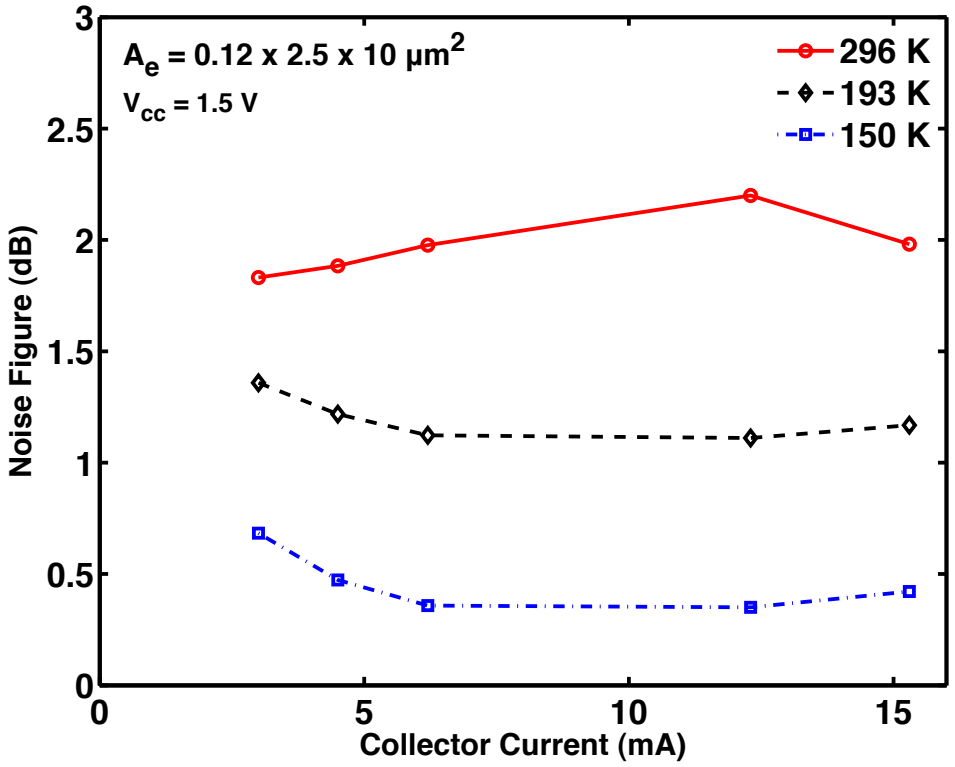


Figure 74: Noise figure of SiGe HBT npn (A_E = 0.12 x 2.5 x 10 μm^2) at 9.5 GHz as a function of collector current for 296, 193, and 150 K.

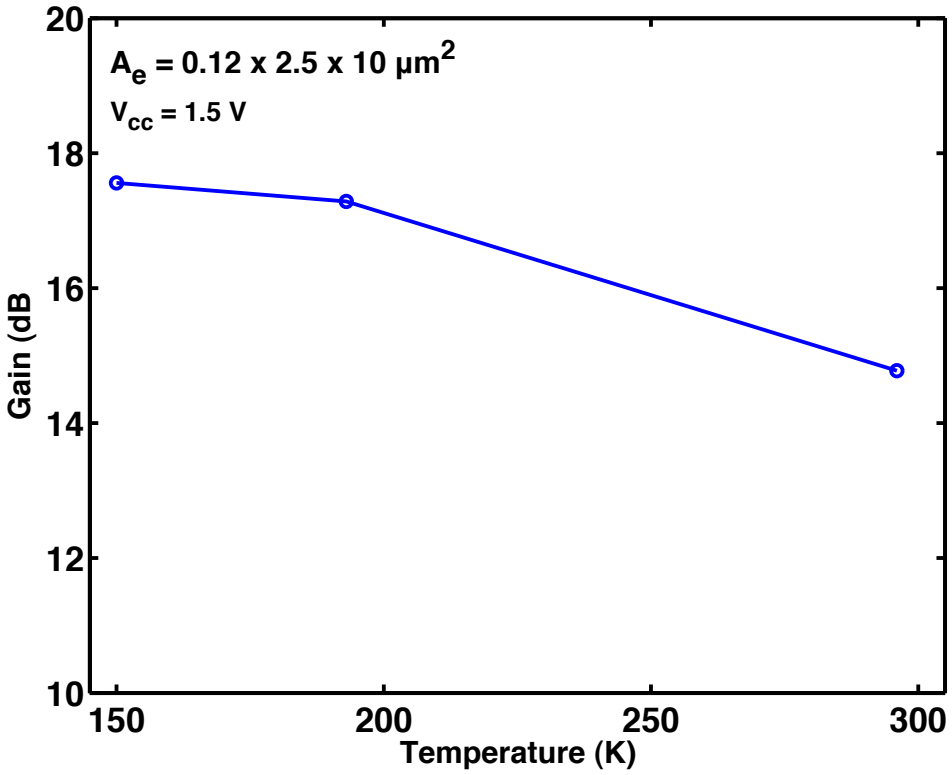


Figure 75: Peak gain of SiGe HBT npn (A_E = 0.12 x 2.5 x 10 μm^2) at 9.5 GHz across collector current as a function of temperature.

to 193 K, and only a small increase in gain from 193 to 150 K, which mimic the results for the LNA performance improvements as shown in the previous section.

The noise figure versus collector current for the npn SiGe HBT is shown in Fig. 74 . For the room temperature measurements at 296 K, the noise figure curve is not as expected; this was determined to be due to a faulty component. The error was only determined during post-processing of the data, however, room temperature noise characteristics of SiGe HBTs has been throughly characterized in [20, 58, 59]. However, the low temperature measurements are as expected across collector current and exhibit minimum noise figure at collector currents between 5 - 10 mA (approximately 2 - 4 mA/μm^2). The SiGe HBT device experiences very low noise figures of 0.5 dB at 150 K, which highlights the very the large performance improvements as the device is operated in cryogenic environments.

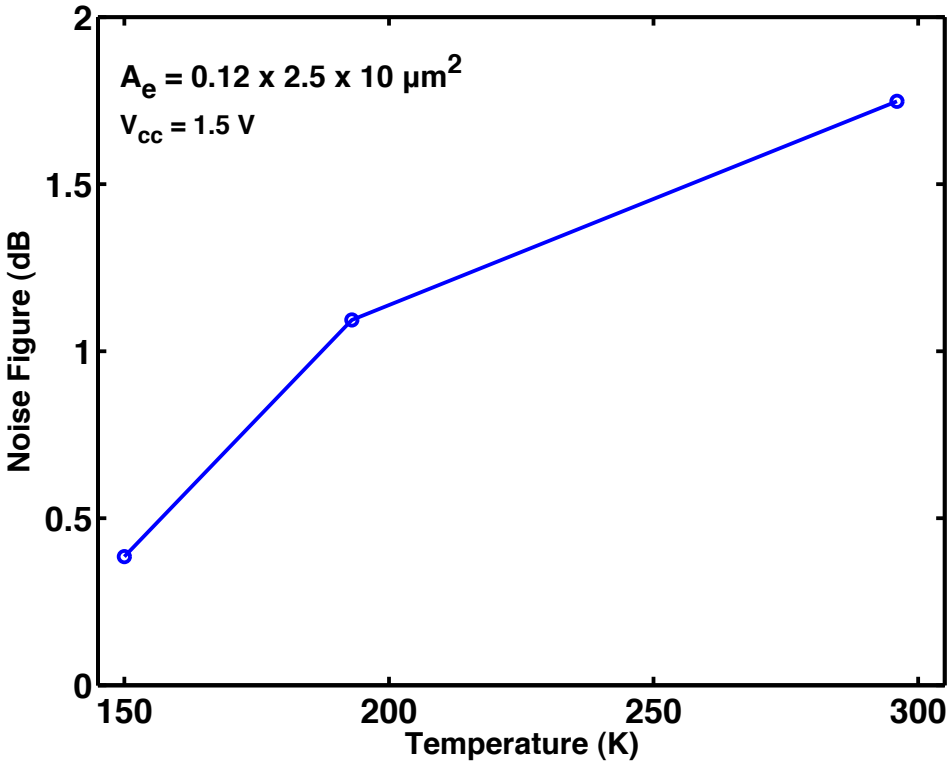


Figure 76: Minimum average noise figure of SiGe HBT npn (A_E = 0.12 x 2.5 x 10 μm^2) across collector current as a function of temperature.

Additional trends can be observed at the device level that match the circuit level response, and are shown in Fig. 75 and 76. In Fig. 75, the peak gain across collector current is plotted at each temperature point. This plot demonstrates that the performance improvements in gain appear to saturate and further cooling will not provide as large of a boost in gain. A slightly different trend is noticed in Fig. 76, where the minimum mean noise figure at 150 K is below 0.5 dB. However, due to ENR uncertainty errors and mismatch, these low noise figure numbers have a larger percentage of uncertainty, but the trends are consistent with the amplifier measurements presented in the previous section.

Using the proposed on-wafer cryogenic noise figure measurements technique, amplifier and device level measurements where conducted and yield results that are consistent with performance improvements as SiGe HBTs are cooled. The technique allows for a straightforward method to calibrate out losses and temperature gradient of these losses to ensure accurate measurements. However, limits of this technique still exist since mismatch and ENR uncertainty are not taken into account, therefore, care should be taken into account to using this technique to ensure valid results.

4.5 Low-Temperature Linearity Characterization

4.5.1 Measurement Setup and Methodology

In section 4.4, an on-wafer noise measurement setup was presented and used to characterize device and circuit noise figure to 150 K. In this section, a two-tone linearity measurement setup is presented based on [46], and modified to include low-temperature operation.

Linearity is an important metric for RF circuit designers as it defines the upper signal limit; this metric coupled with noise figure defines the dynamic range of a amplifier [78]. The two primary metrics to measure linearity are compression point, which measures large-signal linearity; and intermodulation distortion, which

measures small-signal linearity. In this section, a measurement setup for two-tone low-temperature linearity and measured amplifier results are presented.

Intermodulation distortion for an RF system is typical characterized by measuring a common FoM: two-tone third-order intercept (TOI) or third order intercept point (IP_3). To characterize TOI, two sinusoidal tones are injected into the device under test. Due to nonlinearities in the active devices, harmonics and mixing products are created as in the analysis presented in [64]. To understand this phenomenon, a signal is injected into the amplifier, $x(t) = A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)$ then the output would be as shown in Equ. 25:

$$\begin{aligned} y(t) &= \alpha_1(A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)) \\ &\quad + \alpha_2(A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t))^2 \\ &\quad + \alpha_3(A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t))^3. \end{aligned} \tag{25}$$

expanding and simplifying these terms yields the following harmonic mixing terms that are relevant to the two-tone analysis, which are shown in Equ. 26 and 27:

$$\frac{3\alpha_3 A_1^2 A_2}{4} cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^2 A_2}{4} cos(2\omega_1 - \omega_2)t \tag{26}$$

$$\frac{3\alpha_3 A_2^2 A_1}{4} cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_2^2 A_1}{4} cos(2\omega_2 - \omega_1)t \tag{27}$$

For closely spaced fundamental tones, the harmonic products: $2\omega_1 - \omega_2$ and $2\omega_1 - \omega_2$, are of interest due to their proximity to the fundamental frequencies. By analyzing these equations, it can be shown that while the fundamental will behave with a linear response to input power at small signal, where a 1 dB increase in input power will produce a 1 dB increase in output power, the harmonic terms will increase by 3 dB for each 1 dB increase in input power. To find the TOI, the fundamental and third-order intermodulation products (IMD_3) are graphed as function of input power and extrapolated, with the intersection point as the TOI or IP_3, as shown in Fig. 77.

In order to characterize the TOI of an amplifier or a device, two fundamental signal tones are injected into the DUT and these tones along with the third order mixing

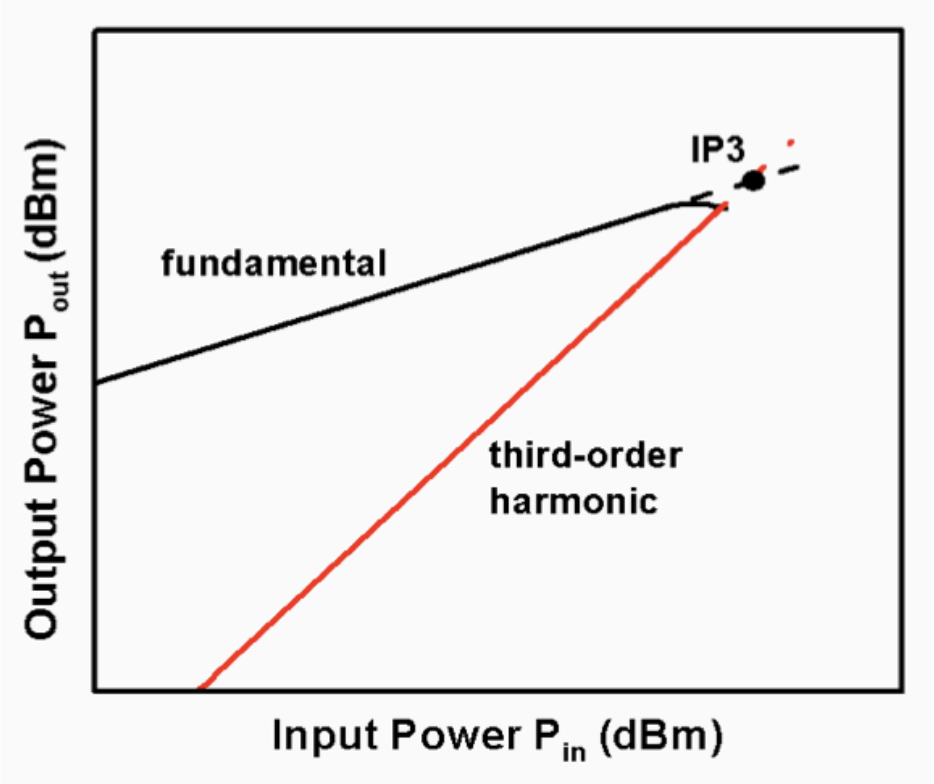


Figure 77: Depiction of third-order intercept point (from [46]).

products are measured at the output, and calibrated back to the DUT reference plane. Since the relationship (1:3) between the fundamental and IMD_3 products are known, output IP_3 can be calculated to be $3/2\ P_{out(fund)} - 1/2\ IMD_3$. Using this technique, only a single measurement point at a specific input power is necessary to determine IP_3. However, in practical measurements, input power should be swept to ensure that the measurement range is above the noise floor and the DUT is in the linear region.

In order to accomplish this measurement, the setup shown in Fig. 78 is used. Most linearity measurement setup require using separate signal generators and spectrum analyzer to generate the input tones and receive the harmonics. In this setup, a network analyzer with a receiver frequency offset feature can be used to generate one fundamental tone and receive all tones, with a standalone signal generator providing the second fundamental tone. In addition, the use of the network analyzer

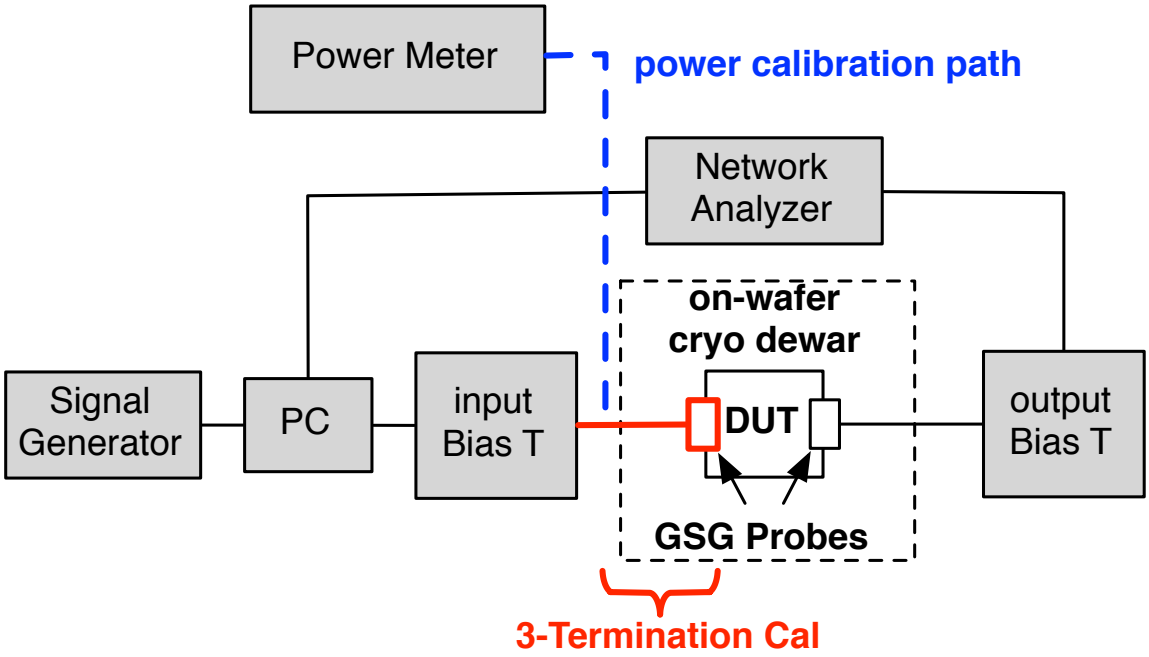


Figure 78: On-wafer cryogenic linearity two-tone measurement setup using a network analyzer as the source and measurement receiver.

allows in-situ S-parameter measurement. The setup can be configured to sweep frequency at a fixed power, or sweep power at fixed fundamental frequencies. For these measurements, the input power was swept to verify linear operation for the DUT.

Similar to the noise measurement setup, the loss of the input block needs to be accurately determined as to calibrate the input power to the DUT reference plane. The 3T calibration can again be used to find the input feedline losses, and combined with a source power calibration to the input of the cryo dewar, the absolute input power to the DUT can be determined. After calibrating the input power, a receiver power calibration can be used to determine the output power at the DUT. Sources of error for this measurement mimic that of room temperature measurement, and therefore, reliable results should be able to be achieved down to deep cryogenic temperatures. However, caution should be taken to ensure that the DUT remains in the linear (small-signal) region at low temperatures. Small-signal operation is typically defined as input powers less than or equal to 3 kT/q (thermal voltage), which

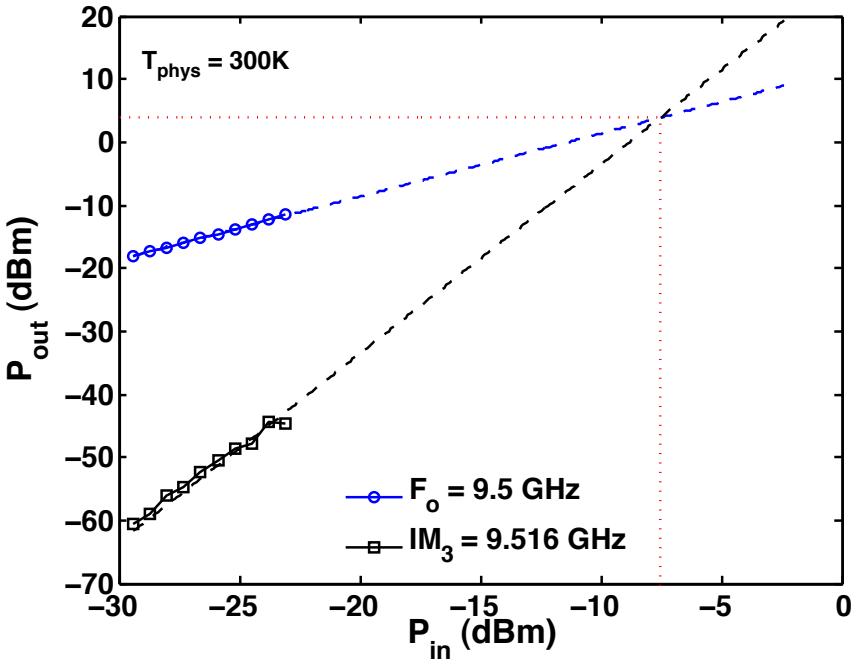


Figure 79: Output power as a function of input power at 300 K for fundamental (9.5 GHz) and IMD_3 (9.516 GHz) showing the extrapolated TOI point for the X-band low-power LNA.

decreases with temperature. So in order to achieve accurate small-signal linearity characteristics, the input power at the DUT should be decreased with temperature.

4.5.2 Results

Using the measurement setup discussed in the previous section, the low-power LNA was characterized at 300, 218, and 173 K. The fundamental tone was chosen to be 9.5 and 9.508 GHz (8 MHz spacing) yielding IMD_3 tones of 9.492 and 9.516 GHz. The *dc* current of the LNA was kept constant at 1.3 mA with a collector voltage of 1.5 V.

Fig. 79 is the room temperature (300 K) linearity result using this measurement setup. Here, the output power is plotted as a function of input power, for the fundamental and third order tones, extrapolated to show the intersection point. For this amplifier, the input TOI is -7.5 with an output TOI of approximately 4 dBm for tones of 9.5 and 9.516 GHz. A linear fit from the two tones verifies the 3:1 slope and the DUT is in the small signal linear region of operation.

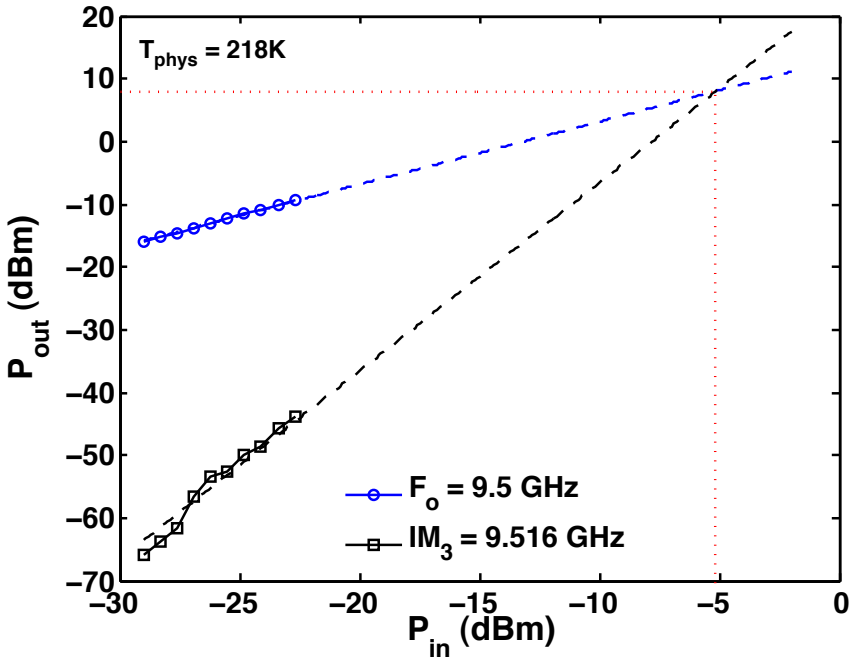


Figure 80: Output power as a function of input power at 218 K for fundamental (9.5 GHz) and IMD_3 (9.516 GHz) showing the extrapolated TOI point for the X-band low-power LNA.

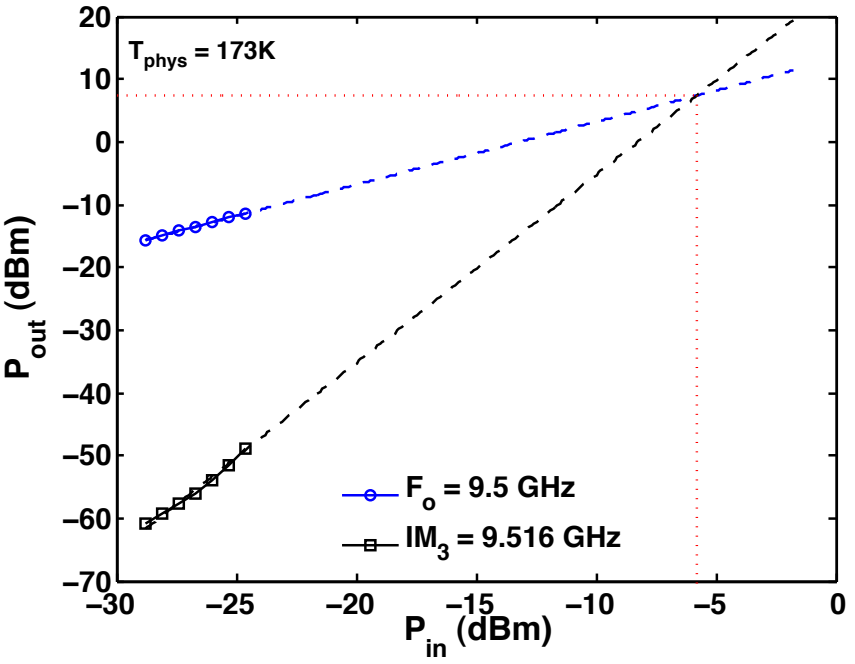


Figure 81: Output power as a function of input power at 173 K for fundamental (9.5 GHz) and IMD_3 (9.516 GHz) showing the extrapolated TOI point.

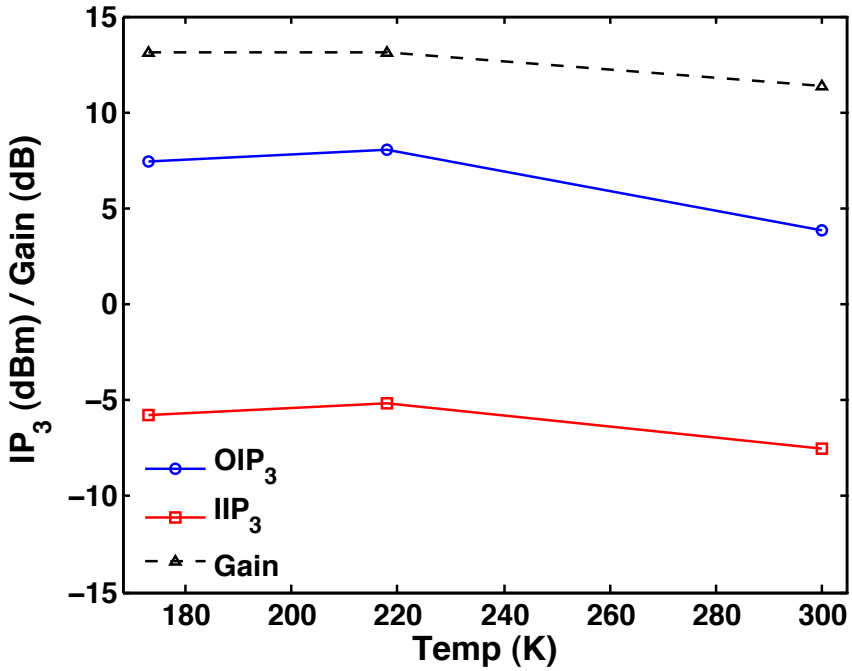


Figure 82: Linearity as function of temperature for low power X-band LNA with an IMD_3 tone at 9.516 GHz.

Two low temperature points were measured at 218 and 173 K and shown in Fig. 80 and 81, respectively. At 218 K, the input TOI increases to -5 dBm and with an increased gain at low temperatures, the OTOI improves to 8 dBm. However, at 173 K, the TOI appears to slightly decrease, with the input TOI falling to approximately -6 dBm, and an output TOI of 7.4 dBm, while the gain remains constant at 13 dB.

Fig. 82 summarizes the linearity results over temperature. From room temperature to 218 K, there is a clear improvement in linearity. However, from 218 to 173 K, no improvement is measured, and the trend appears for the linearity to decrease. In [33], linearity of first generation SiGe HBTs are explored and was shown to be a function of the collector design, with degraded linearity for HBTs without a selectively implanted collector. In addition, since the bias currents were held constant across temperature and since the device peak f_T current increases at lower temperature, the optimal linearity point might require a slightly higher bias, which might explain the decrease in linearity at this lower bias point.

4.6 Summary

In this section, low temperature RF characteristics of both SiGe HBT devices and circuits have been characterized down to temperatures as low as 15 K. Two packaged LNAs were characterized in a custom designed cyrogenic noise measurement dewar, and shown to have noise temperatures of less than 21 K. Noise figure of SiGe HBT devices and a low-power LNA was measured using a proposed on-wafer measurement setup, that allows for 50 Ω measurements in a cryogenic dewar. The proposed setup accounts for input and output losses using a "3T" calibration technique and by using a passive resistor divider structure, is able to provide temperature correction to achieve accurate noise figure measurement. The third generation SiGe HBT device was measured to have a noise figure of approximately 0.5 dB at 150 K, which is a decrease in over 1 dB from the room temperature results. Similar results were measured on a low-power X-band LNA, which also exhibits an over 1 dB decrease in noise figure from room temperature (2 dB NF) to 193 K (1 dB). These results are are consistent with the expected improved noise performance of SiGe HBTs at low temperature.

Two-tone linearity at X-band of the low-power LNA was also characterized down to 173 K. A custom on-wafer measurement setup using a signal generator and network analyzer to provide the two-tone input signals and receive the fundamental and third harmonic signals. To calibrate the losses in the dewar, the "3T" calibration procedure is used to characterize the input feed line. The input TOI was shown to improve from -7.5 dBm at 300 K to -5 dBm at 218 K, however, the linearity falls slightly to -6 dBm at 173 K. This decrease in linearity could be due to increased non-linearity as the HBT is cooled. In addition, since the current bias of the LNA was held constant, the optimal linearity point might shift to higher current levels to match the optimal peak f_T point.

A proposed on-wafer cryogenic measurement setup for noise figure and linearity were outlined, and measured results of SiGe HBT devices and circuits were verified

across temperature. On-wafer measurement allow for simplified device and circuit testing, since custom packages are not needed. In addition, multiple geometries, as well as different devices maybe characterized during one measurement cooling cycle, greatly improving the ability gather ample data to accurately model SiGe HBTs at wide-temperatures.

CHAPTER V

INVESTIGATION OF RADIATION EFFECTS ON T/R MODULE CIRCUIT BLOCKS

5.1 Total Ionizing Dose Phase Shifter Irradiation

5.1.1 Introduction

Phase shifters are a critical piece in T/R modules for phased-array antenna systems since they provide the ability to electronically steer the antenna beam. Even small degradations (i.e. few degrees increase in phase error) in this circuit could cause large changes in antenna performance, therefore it is very important to understand radiation response of these phase shifters enabling their use in space environments. Other Si-based analog and RF circuits including LNAs, voltage controlled oscillators (VCOs), and band-gap references (BGRs) have been shown to be radiation tolerant as highlighted in [18, 43, 74] . Historically, phase shifter performance in a radiation environment has been a relevant topic as noted in [9], which reports on the results of neutron irradiation of PIN diodes used in phase shifters. High-frequency circuits for space-based phased-array radars have been demonstrated in p-HEMT technology [70], however, no study of Si-based phase shifters in a radiation environment has been conducted to date.

The two irradiated phase shifters are based on an X-band (8 GHz - 12 GHz), 4-bit, switched high/low-pass filter topology. The first variant uses a diode-connected SiGe HBT as the RF switching device in a BiCMOS series-shunt SPDT switch. The other phase shifter variant uses n-channel CMOS devices in a "pass-gate" configuration as the series-shunt SPDT switch. Block diagrams of both phase shifters are shown in Fig. 83. The optimum ordering of the bits and a detailed design of the phase

shifter and switches are discussed further in [14, 42, 50]. Some key figures-of-merit for phase shifters are number of bits, insertion loss, phase error, and dissipated power. The number of bits, n, determines the number of phase-states (2^n) and controls the antenna pattern and sidelobe levels. The insertion loss impacts receiver sensitivity, while phase error will cause disruptions in the antenna pattern. Phase error for large array panels is a critical metric since a small increase in error could dramatically change the antenna pattern, increasing side lobe levels, and degrade antenna performance. Dissipated power is another important metric since for large phased-array systems many thousands of T/R modules are often necessary.

This study on phase shifters is necessary because their radiation response cannot be directly inferred from typical device level radiation studies as the transistors are not usually irradiated in this operating condition (diode-connected or pass-gate operation) therefore the circuit level radiation response is not necessarily obvious. For example, radiation induced damage to the gate oxide in an n-MOSFET device could change the device parasitic capacitances, changing the SPDT return loss greatly degrading phase error. In addition, the eight series SPDT switches magnify any degradation, which could severely impact phase shifter performance given only a small change to the SPDT, therefore, understanding the radiation response of these circuits are crucial for their use in space applications.

The phase shifters were fabricated in the commercially-available IBM 8HP SiGe BiCMOS process which contains 0.13 μm CMOS and a third-generation SiGe HBT with f_T/ f_{MAX} of 200/250 GHz [65]. The SiGe HBT phase shifter has lower insertion loss than the CMOS phase shifter; however, the HBT version consumes considerably more power since the HBT switches require current to operate. This study indicates that both SiGe HBT and CMOS phase shifters are radiation tolerant up to 3 Mrad total dose (SiO_2) of protons with negligible changes in RF performance. The radiation tolerance is derived from a combination of the operating regimes of the transistors

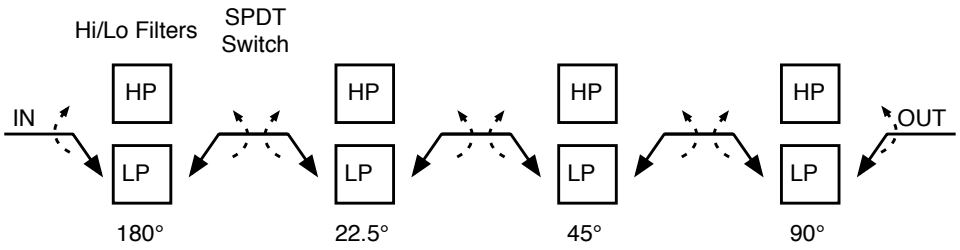


Figure 83: 4-bit phase shifter topology consisting of single-pole double throw (SPDT) switches and high-pass / low-pass filter sections.

and the relative insensitivity to small bias changes in the RF performance of the switches.

5.1.2 Circuit Design and Topology

The two main elements in both phase shifters are SPDT switches and high/low-pass filter sections as highlighted in Fig. 83. Each phase shifter has four "bits" each containing two SPDT switches and a high and low-pass filter section. Each bit has a fixed phase difference (22.5, 45, 90, or 180 degrees) between each filter, allowing a total of 16 achievable phase states. Each filter section is switched into the RF path using the SPDT switches by a digital control signal. Micrographs of both phase shifters are highlighted in Fig. 84. The filter sections consist of passive elements (spiral inductors and capacitors) and therefore any radiation damage is assumed to be negligible [18]. The SPDT switches, however, contain transistors and will most likely be the source of any performance degradation. The switch insertion loss is attributed to the 'r_{on}' and capacitances associated with the switching devices. Therefore, if irradiation of these circuits increases 'r_{on}', the total insertion loss will increase, thereby degrading the overall phase shifter performance.

The SPDT switches used in the CMOS phase shifter consist of a series n-MOSFET transistor (M_1 and M_2) used as a "pass-gate" to act as the switch (Fig. 85). S and $\bar{S}$ are buffered through digital inverter stages (not shown). The CMOS phase shifter dissipates only leakage current when operating, since both the source and drain

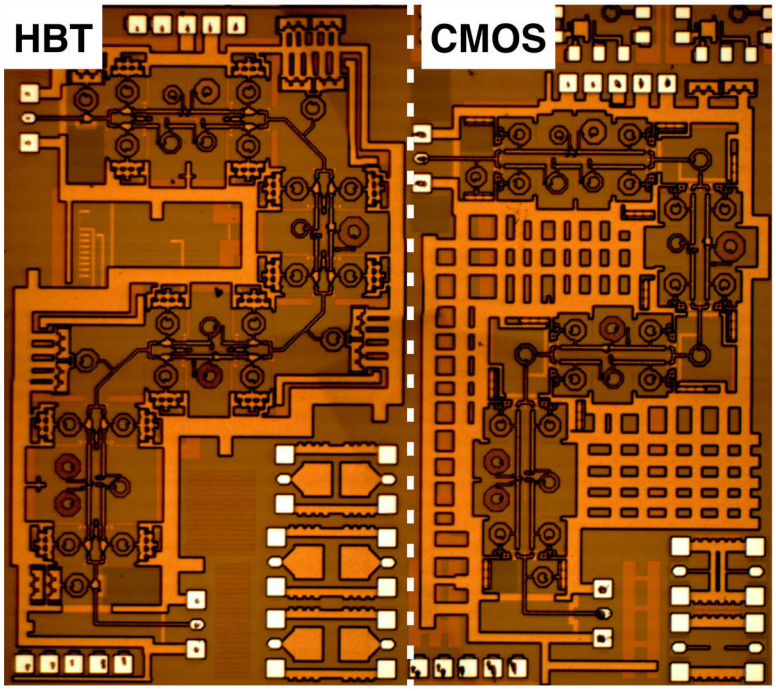


Figure 84: Micrograph of the SiGe HBT (left) and CMOS (right) phase shifters.

potentials of the pass-gate switch are not biased. For each switch, the gate of the series n-MOSFET device is switched from 1.2 V ("on") to 0 V ("off").

The SiGe HBT SPDT switch is configured differently due to the bias requirements for the SiGe HBTs (Fig. 86). The series HBTs (Q_1 and Q_2) are diode-connected and act as the switch, while the shunt-connected p-MOSFET devices (M_1 and M_2) are used to increase isolation . Devices Q_3-Q_6 are a 5 to 1 current mirror to bias the diode-connected SiGe HBTs and M_3-M_6 digitally control to the switch. The current, *ibias*, is supplied by a p-MOSFET current mirror (not shown) to distribute stable current references for all of the switches in the phase shifter. When S is high, the current mirror for Q_2 is "off", and the diode is shorted while Q_1 is turned "on" and the switch is set to the low-pass filter section. The switching is accomplished by steering the current from the high-pass path to the low-pass path, differing from the CMOS SPDT which is switched using only the gate voltage. Inverter stages similar to the circuits in the CMOS phase shifter were used to generate the S and $\bar{S}$ signals.

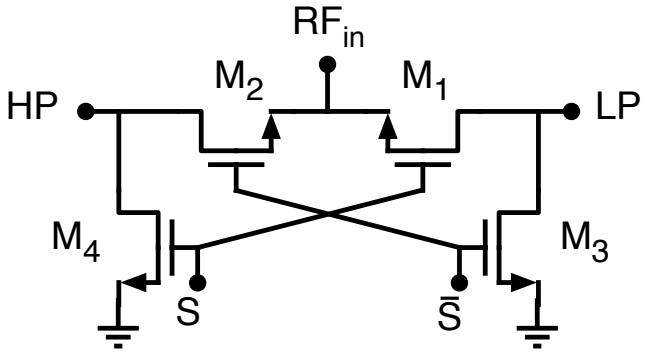


Figure 85: Single-pole double throw switch topology used in CMOS phase shifter.

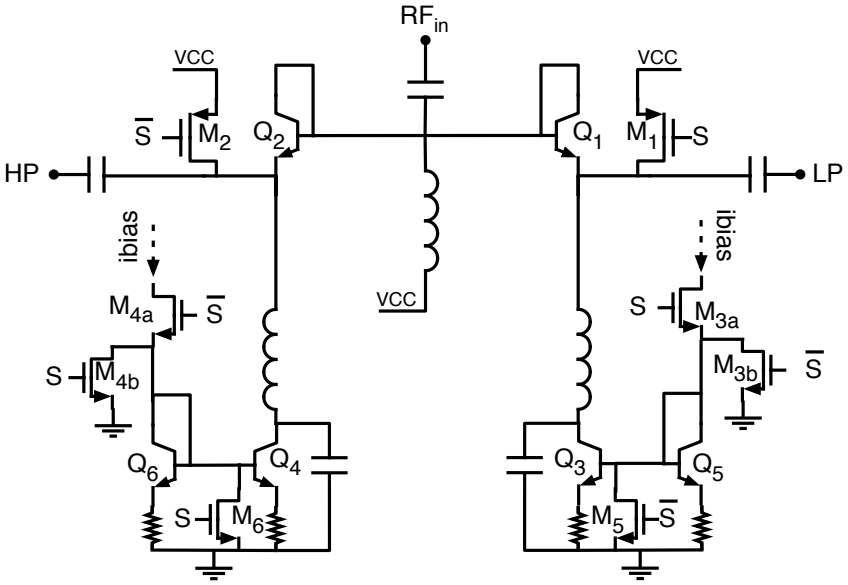


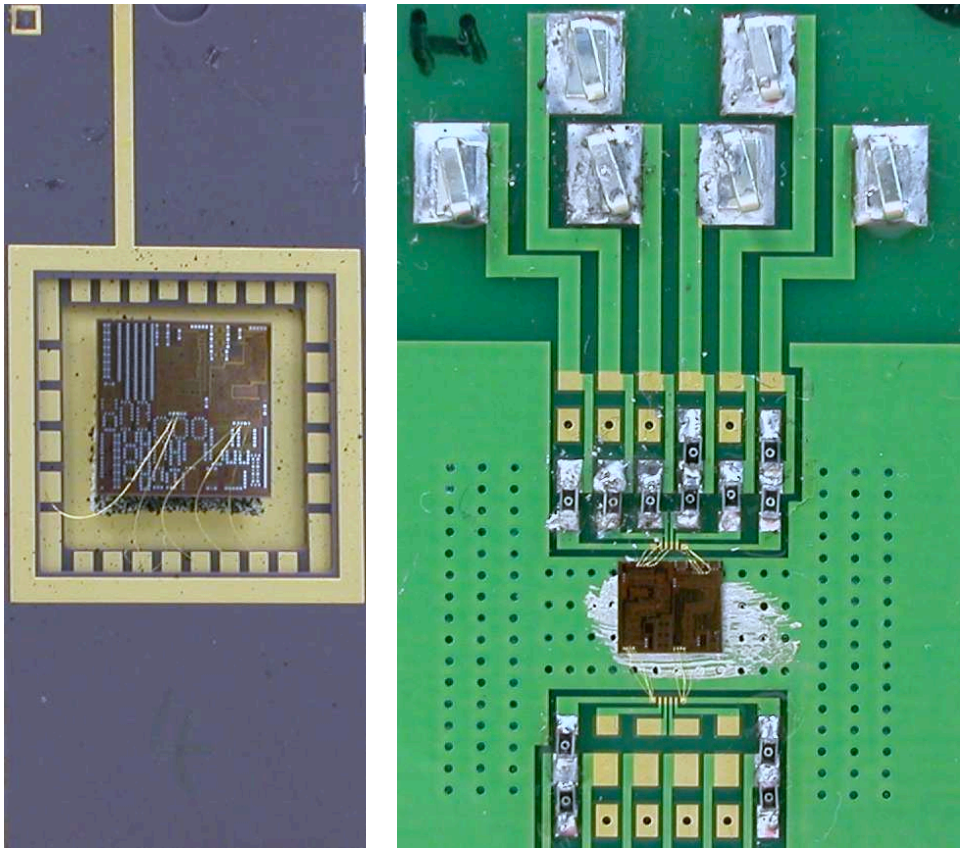
Figure 86: Single-pole double throw switch topology used in SiGe HBT phase shifter.

5.1.3 Experiment Setup and Test Conditions

Two experiments were conducted on the phase shifters, with the first set of phase shifters irradiated at room temperature using space-relevant 63.3 MeV protons, at a dose rate of 1 krad(SiO_2)/s, yielding a maximum total dose of 100 krad (SiO_2). The second set of phase shifters were irradiated under the same conditions, but to higher dose levels of 500 krad, 1 Mrad, and 3 Mrad. Both irradiations were performed at the Crocker Nuclear Laboratory at the University of California at Davis, and the radiation setup has been previously described in [69]. All phase shifters were biased to their *dc* operating points during exposure; however, the measurement fixtures for both experiments differed.

For the first set of phase shifter irradiations (to 100 krad), a novel method was used to bias these high frequency RF circuits in beam. The phase shifters were originally designed for and tested using on-wafer measurements, and therefore an expensive RF package would have been necessary to provide bias in the proton beam during exposure. Instead, the phase shifters were mounted in a standard (cheap) 28-pin dual in-line package (DIP) with only the *dc* bondpads wirebonded to the package (Fig. 87a.). The devices were characterized in package using the high-frequency probes to measure the pre/post-radiated RF performance. The advantage of this experimental approach is that no expensive custom RF package was needed.

The second experiment was also conducted at the Crocker Nuclear Laboratory; however, a different measurement fixture was used to bias the devices and additional total dose levels of 500 krad, 1 Mrad, and 3 Mrad were tested. For this experiment, the phase shifters were mounted on an inexpensive custom-designed FR-4 board that allowed the north and south *dc* connections of the phase shifter to be wire-bonded to the board while still allowing for on-wafer probing for the input and output high-frequency signals (Fig. 87b). This setup allowed for less series resistance for the *dc* connections over the previous setup and was better-suited for the HBT phase shifter,



(a) **(b)**

Figure 87: (a) Package used to supply *dc* bias for 100 krad irradiation, (b) Board used during irradiation to 500 krad, 1 Mrad, and 3 Mrad.

which operates at much higher current levels. In addition, this setup proved more robust for on-wafer measurements since it could be easily mounted on a standard high-frequency probe-station chuck.

In total, seven phase shifters were irradiated, four using the DIP setup (to 100 krad), and three using the board setup (0.5 - 3 Mrad). The RF performance of the phase shifters were measured using an Agilent E8363B PNA while *dc* biasing was performed using an Agilent 4155C semiconductor parameter analyzer. All circuits were biased to their standard operating points: for the SiGe HBT phase shifter, V_{CC} = 2 V, I_C = 80 mA, while for the CMOS phase shifter, V_{DD} = 1.2 V and I_D = 0.26 μA.

5.1.4 Post-Irradiation Phase Shifter Performance

For both experiments (100 krad and 0.5 - 3 Mrad), the *dc* current for the CMOS phase shifter increases; while for the HBT phase shifter the current was shown to decrease. Fig. 88 plots the percentage change in bias current for total doses of 0.5, 1, and 3 Mrad. A clear correlation between the percentage change in bias current for the CMOS phase shifter is apparent; however, no such trend can be seen for the SiGe-HBT based circuit. In addition, even though the MOS phase shifter shows a much higher percentage change in current, the absolute change in current is much lower than the HBT phase shifter since the bias current is considerably smaller.

Since the CMOS SPDT switches in the phase shifter do not consume any power, the bias currents are attributed to the leakage currents passed through the inverters driving the gates of the n-MOSFETS. Therefore, it is reasonable to assume that irradiation causes the n-MOSFETs leakage currents to increase, driving the increase in the bias current for the CMOS phase shifter. However, for the SiGe HBT based phase shifter, the circuit is more complex due to the biasing requirements for the HBT switches, and further discussion is provided in Section 5.1.5.

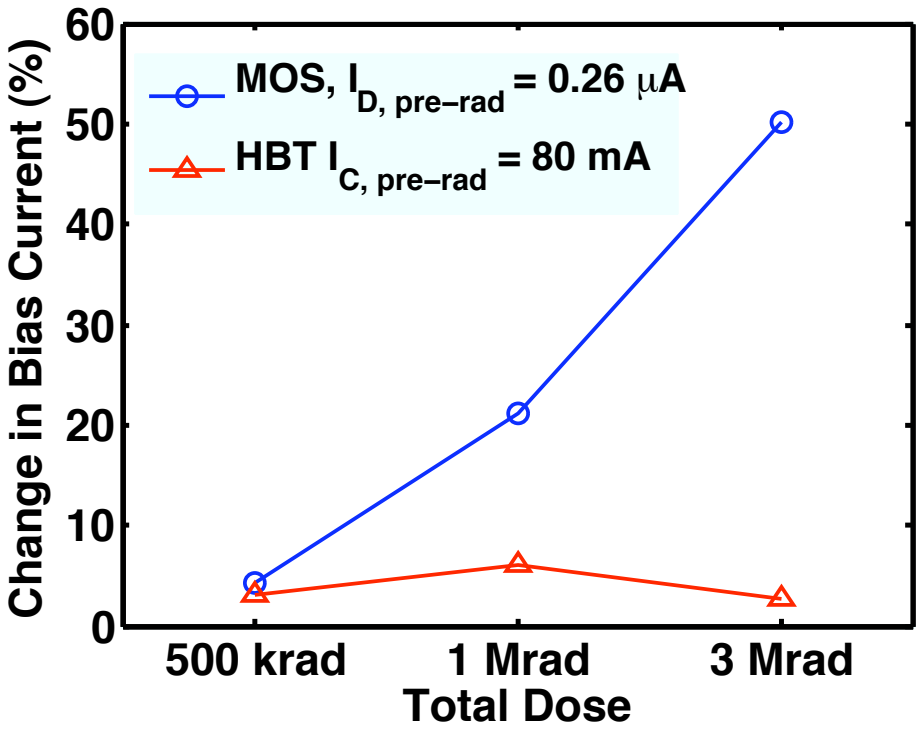


Figure 88: Change in bias current of both MOS and HBT phase shifters for each total dose point.

Even though noticeable *dc* performance changes were observed between pre- and post-irradiation measurements, the RF performance of both phase shifters shows only a negligible change. The measured RF performance of the 100 krad exposure are shown in Fig. 89, which plots pre- and post-irradiation S_{21} at the nominal (lowest) phase shifter state setting, 0000. These results show only a moderate change in insertion loss with radiation exposure, and is within measurement error.

Another important figure-of-merit for phase shifter performance is the RMS phase error, which gauges the relative error between the phase states (a large RMS phase error would reduce the ability to scan the phased-array antenna). For the 100 krad irradiation, the 16 phase states of the phase shifters were measured pre- and post-irradiation and Fig. 90 highlights the CMOS phase shifter performance. The RMS phase error can be calculated from these data, and shows little change for both phase shifters, as highlighted in Fig. 91.

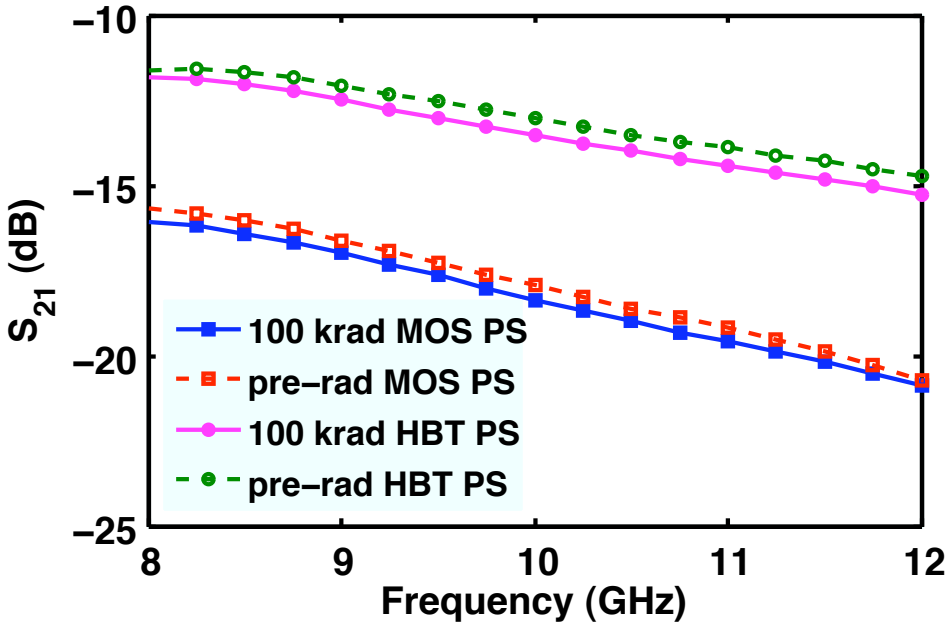


Figure 89: Comparison between CMOS and SiGe HBT pre- and 100 krad irradiation S_{21} response at phase state 0000.

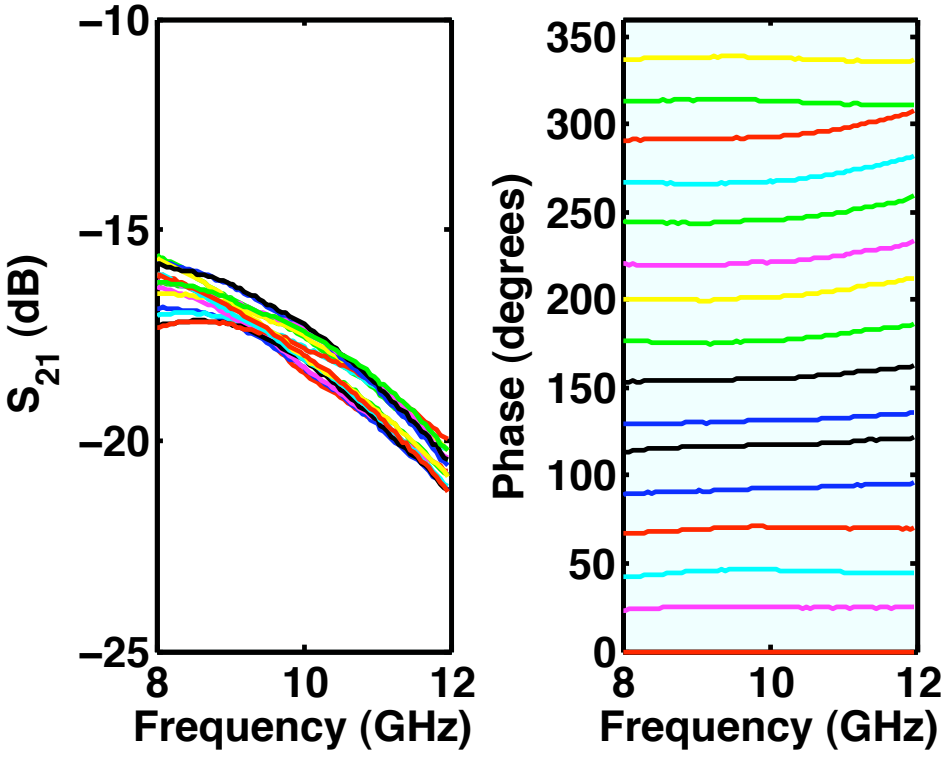


Figure 90: CMOS phase shifter S_{21} and phase across the 16 states after 100 krad total dose exposure.

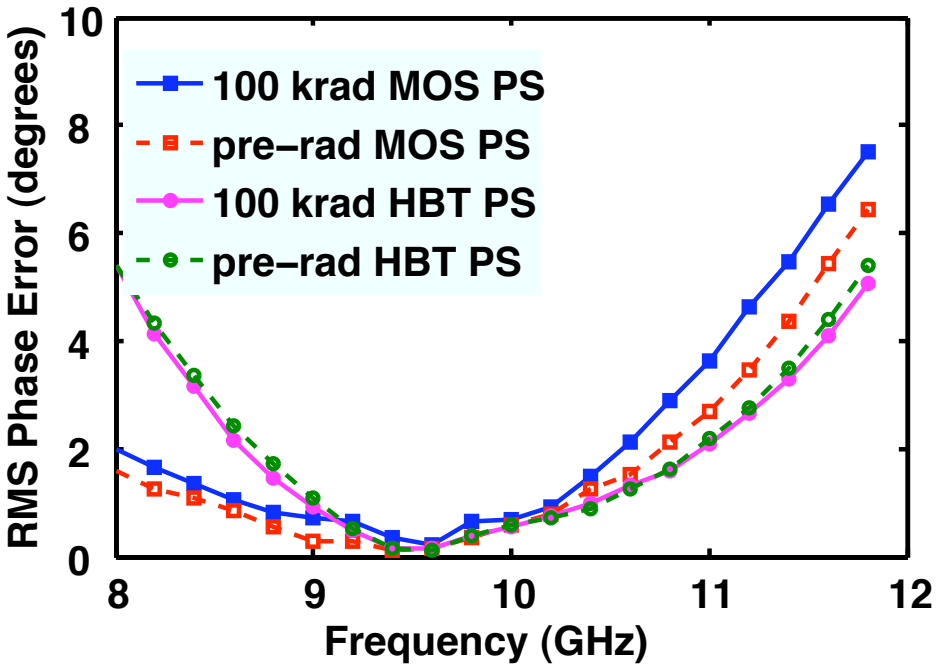


Figure 91: RMS phase error for the CMOS and SiGe HBT phase shifters pre- and post-irradiation for the 100 krad exposure.

The second radiation experiment to total doses of 500 krad, 1 Mrad, and 3 Mrad show similar results to the 100 krad experiment. Fig. 92 highlights insertion loss for the each phase shifter pre- and post-irradiation, showing negligible change for both phase shifters, even up to 3 Mrad total dose with the observed change in S_{21} well within measurement tolerances. These results indicate that both the CMOS and HBT phase shifters are tolerant up to 3 Mrad total dose exposure, more than adequate for most orbital applications.

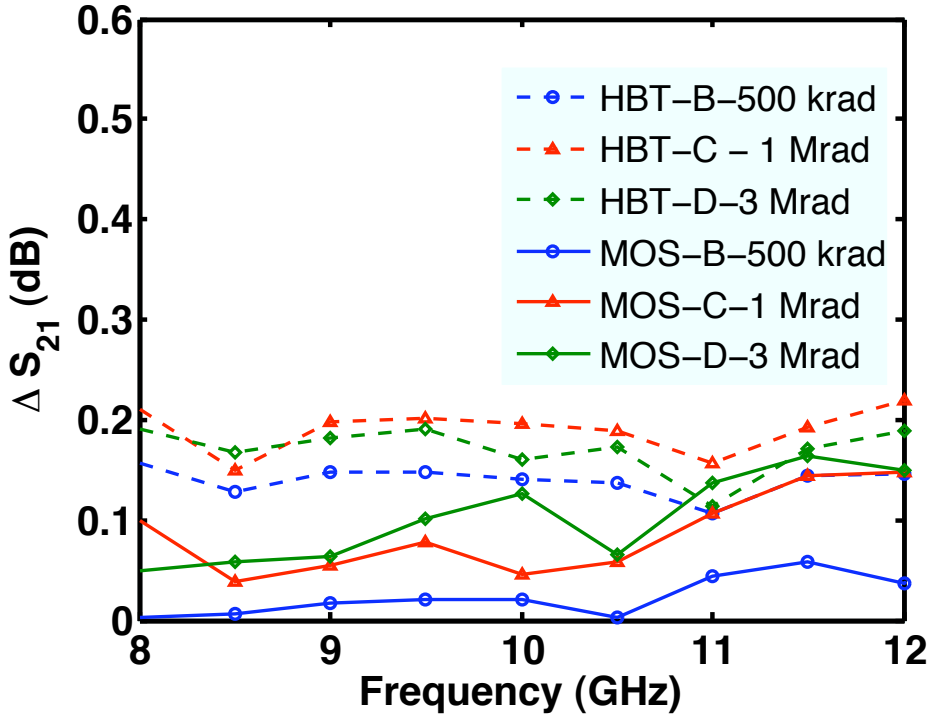


Figure 92: Change in insertion loss between pre- and post-irradiation of 500 krad, 1 Mrad, and 3 Mrad for both MOS and HBT phase shifters.

5.1.5 Discussion

Even though only slight changes were observed between the pre- and post-irradiated samples for all doses tested, an understanding of how these circuits are affected by a radiation environment can be achieved through circuit simulations. Another goal of these simulations is to understand how the noticeable changes in *dc* currents have no impact on RF performance of either phase shifter. In addition to answering why neither phase shifter showed any noticeable RF performance degradation, simulation results can reveal the limits of phase shifter total dose tolerance.

In order to mimic the effects of radiation-induced damage on these phase shifters, the specific circuit topologies and knowledge of radiation effects on these transistors were analyzed. Extensive investigation of the SiGe HBT radiation response as highlighted in [19] shows little damage for normal operating bias currents and only minor changes to its high frequency performance [17]. Therefore, we do not expect these devices to be a source of concern for the irradiation of the phase shifters. However, as discussed in [87], these 130 nm n-MOSFETs do show significant off-state leakage currents which could in principle affect the phase shifter performance.

For these simulations, this leakage current was modeled in a Cadence simulation environment by including an ideal current source from drain to source for all relevant n-MOSFET devices. This leakage current was swept and the corresponding *dc* and RF performance changes were analyzed. The range of simulated leakage currents (to 50 μA) is considerably greater than what would typically be achieved through irradiation, a 1 Mrad total dose is expected to increase the off-state leakage for an n-MOSFET device to only 0.1 μA [34]. However, it is still instructive to examine the effects of such extreme changes on circuit performance since it allows a greater understanding of the sensitivity of circuit performance to an increase in leakage.

For the CMOS phase shifter, the key device most strongly affected by the increased leakage current would be the n-MOSFET device in the inverters used to buffer the

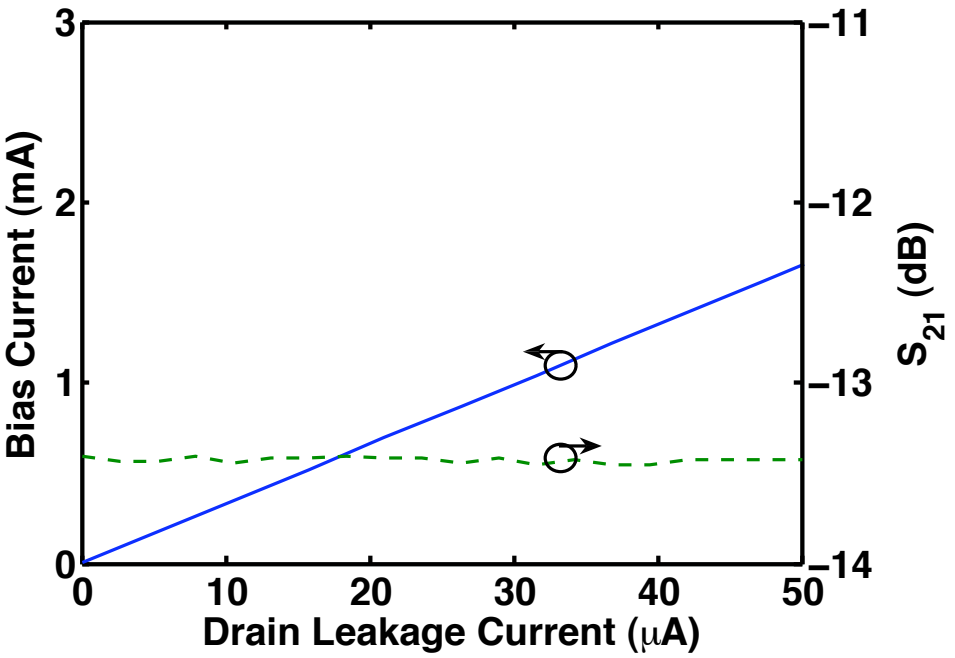


Figure 93: Simulated results of the MOS phase shifter bias current and insertion loss at 10 GHz as a function of radiation induced leakage.

control signal to the SPDT switches [34]. Fig. 93 plots bias current and insertion loss changes as a function of an increase in leakage current in all of the inverters used in the CMOS phase shifter.

It is clear from these simulations that a slight increase in leakage current will cause a large change in bias current due to the many inverters used to generate the control signals for each switch. Even though this current does change considerably, no change is seen in the simulated insertion loss. These simulated results agree with the measured data, highlighting the probable cause of the increase in the CMOS phase shifter bias current, while no RF performance degradation was measured. However, these simulations only model ideal leakage currents and therefore further analysis on the performance degradation due to irradiation of n-MOSFETs in a pass-gate configuration is necessary.

Similar simulations can be performed for the HBT phase shifter; however, due to the more complex bias and switching scheme needed for the HBT SPDT switches, the

various n-MOSFET devices could impact the phase shifter performance differently. To analyze the influence of the various devices, leakage components were selectively added to the simulations, yielding four different simulation conditions, highlighted in Table 7. Fig. 94 shows the simulated *dc* and RF performance of the HBT phase shifter under these simulation conditions. A decrease in phase shifter bias current as the leakage current is increased under all of the four conditions simulated. This decrease is due to the n-MOSFETs degrading the operation of the 5 to 1 current mirror for biasing the diode-connected HBT series switch, causing its bias current to decrease. Conditions one through three show a steady decrease with increase leakage current; however, adding inverter leakage in condition four shows a slight increase in bias current over condition three due to the additional current drawn by the inverters.

Even though the currents in the devices are changing, there is only a minimal degradation in phase shifter insertion loss, and at very low leakage levels, such as those achievable at 3 Mrad total dose, almost no change would be present in the RF performance, as confirmed by the measured results presented in this work. However, with simulations to very high leakage levels, the HBT phase shifter does show a leakage dependent RF performance due to the radiation damage in the bias network. This surprising result is counterintuitive to what is typically understood as SiGe HBT circuits having greater TID immunity than CMOS based circuits. In addition, if the current mirror ratio of the SiGe HBT SPDT switch is increased to 20 to 1 to minimize power dissipation, the effect of the shunt n-MOSFET leakage will have even a greater impact on the RF performance of the phase shifter. This impact on the HBT based phase shifter can be mitigated or eliminated by altering the bias network and control scheme to remove n-MOSFET devices from these critical nodes, if needed.

Table 7: Leakage Conditions for n-MOSFET Devicein HBT Phase Shifter

Condition	modeled n-MOSFET leakage[1]
1	M_5 and M_6
2	M_3 and M_4
3	M_3 - M_6
4	M_3 - M_6 and inverters

1. Devices labels refer to Fig. 86.

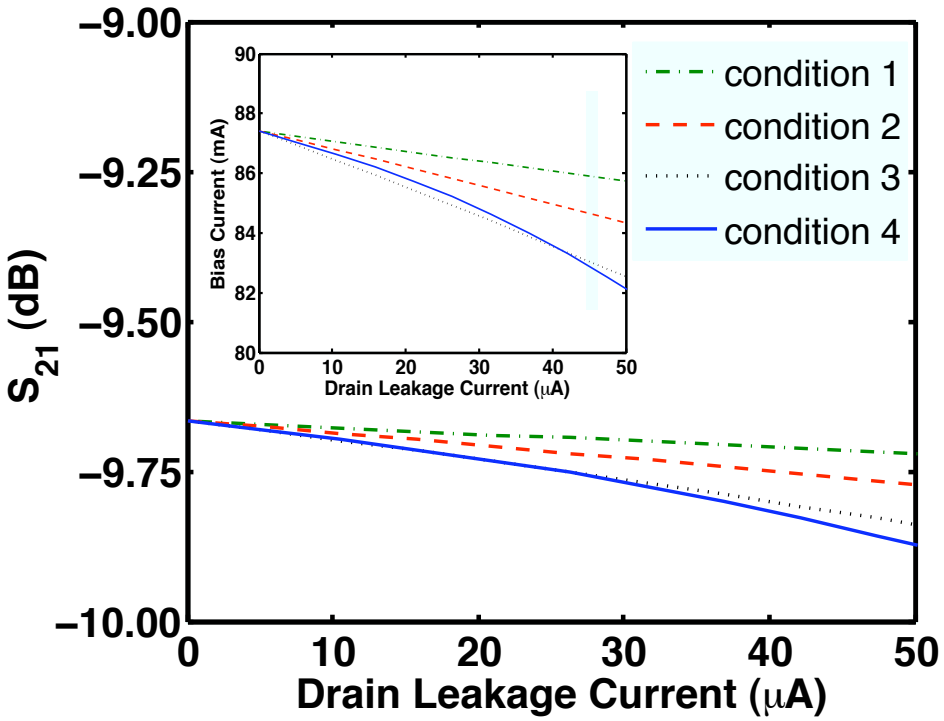


Figure 94: Simulated results of HBT phase shifter insertion loss at 10 GHz as a function of radiation induced leakage for various leakage conditions with inset highlighting simulated *dc* performance changes.

5.1.6 Summary

These results highlight the radiation response from two Si-based phase-shifters used in next generation phased-array antennas. Both SiGe HBT and CMOS phase shifters showed acceptable tolerance up to 3 Mrad of total dose exposure with only slight changes in *dc* supply currents, and no significant changes to RF performance. In addition, we highlight two low cost measurement approaches to allow for biasing high-frequency circuits in a radiation environment, one using a standard 28-pin DIP, and the other using a inexpensive FR-4 board.

To further understand the impact of the irradiation on the phase shifters, circuit simulations mimicking radiation-induced leakage were performed and proved to be consistent with the measured data. For the CMOS phase shifter, no change RF performance is expected due to radiation-induced leakage current since the circuit is not sensitive to changes in bias currents. It can be inferred that the radiation damage to the gate oxide does not impact the RF performance of the n-MOSFET device severely enough to cause degradation of the SPDT switches. The HBT phase shifter will experience changes to its RF performance as leakage currents increase; however, these effects can be mitigated by modifying the bias and control networks and thus making the HBT phase shifter also immune to effects of total dose radiation. This work is the first step in demonstrating that CMOS and SiGe HBT based phase shifters can be used in a space environment, specifically that CMOS phase shifters utilizing n-MOSFET devices are still TID tolerant even though the devices themselves have been shown to have significant TID response.

In the next section, single-event effects (SEE) on SiGe HBT devices used in T/R module digital blocks are investigated. In addition, a novel device topology is presented that aims to mitigate SEE in these circuits.

5.2 Novel Radiation Hardening by Design Technique for Single Event Effect Mitigation

5.2.1 Introduction

Digital blocks in active T/R modules provide control for RF and analog circuit components and allow serial control of functions such as beamsteering, transmit/receive switching, and gain control through a serial-to-parallel ASIC. Electronics operating under radiation exposure can and do suffer disruptions and degradation that can ultimately induce system failures [68]. Radiation induced errors in these digital blocks could lead to damage of the T/R module, degrading antenna performance. Typically, solutions for preventing these radiation-induced failures rely on either process modifications (radiation hardening by process - RHBP), or device layout, circuit and/or system design modifications (radiation hardening by design - RHBD). RHBP is undesirable due to the increased fabrication costs, while RHBD techniques typically require significantly more power and area to achieve acceptable levels of radiation tolerance (e.g., a classical RHBD approach is triple modular redundancy - TMR [39]).

The "Holy Grail" in space electronics is the development of digital circuits that can withstand the space environment with no added cost, area or power penalty. A particularly difficult radiation effect to harden against is single-event upset (SEU), where impinging heavy ions (at energies too high to shield) deposit charge in the semiconductor [49]. This charge is then swept to sensitive circuit nodes, causing transient voltage and/or current signals that can propagate to the circuit output and induce bit errors in digital systems [17]. Conventional SiGe HBTs, which are fabricated on bulk substrates, while total ionizing dose (TID) hard as fabricated, are well-known to suffer from SEU sensitivity [49, 57].

A novel SiGe HBT layout topology, the inverse-mode cascode (IMC) SiGe HBT, represents a simple RHBD approach for SEU mitigation in SiGe logic, and appears to have the potential for improved SEU tolerance, with little or no power, area, or cost

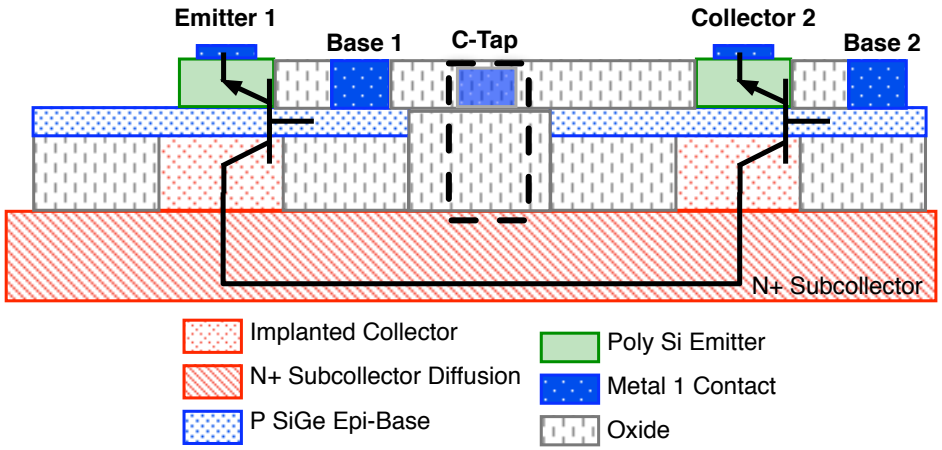


Figure 95: Profile of inverse-mode cascode (IMC) SiGe HBT with shared sub-collector (from [63]).

penalty [63, 76]. In the present work, digital blocks, which could be integrated into T/R modules, are used to explore the implementation of the IMC SiGe HBT using simple TMR-less circuit topologies to fully exploit the SEU mitigation potential of this new RHBD approach. Transient ion microbeam data is presented, showing the efficacy of the IMC SiGe HBT, and demonstrate that Gb/s IMC SiGe logic can be achieved. To understand the IMC's SEU benefits, shift registers (SR) were tested in a heavy-ion beam to determine the error cross section of these circuits.

5.2.2 IMC Device Topology

The IMC SiGe HBT device uses an inverse-mode SiGe HBT (emitter and collector swapped) in a cascode topology to separate the output node of the cascoded devices from the sub-collector. Fig. 95 depicts the profile of an IMC SiGe HBT with a shared sub-collector. Despite the use of a device operating in inverse-mode, the IMC still achieves ample performance for high-speed circuits, with cutoff frequency (f_T) exceeding 100 GHz for a third-generation IMC SiGe HBT, while maintaining its total dose radiation tolerance. In addition, the third-generation IMC device area was not increased over a standard (C-B-E-B-C) *npn* device layout, as shown in Fig 96.

In [63], the C-tap node (Fig. 95) was demonstrated to shunt charge away from

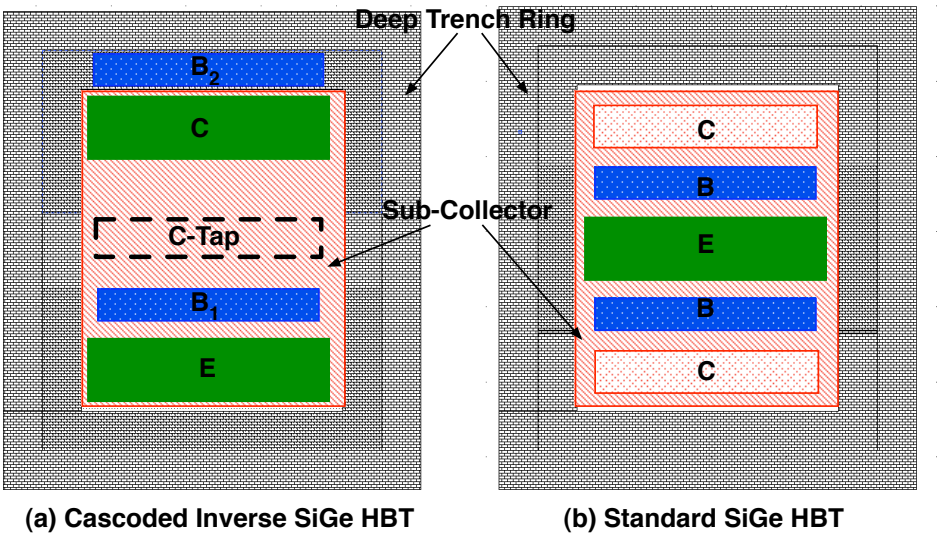


Figure 96: Layout of third-generation IMC device (a) compared with a standard (C-B-E-B-C) SiGe HBT (b) (from [63]).

the output node, potentially improving single event response. In [76], a capacitor connected to the C-tap node was simulated to similarly reduce the collector current transients. Therefore, the key to achieving SEU hardness using this device is to provide a path to remove excess charge from the sub-collector. As shown in Fig. 97, an n-Tiedown (a minimal-sized parasitic diode of an n+ to p-substrate contact) allows for such a connection to be easily made with minimal area overhead. To verify the benefits of using an n-Tiedown IMC RHBD scheme, time resolved ion beam induced charge collection (TRIBICC) testing was performed at Sandia National Laboratory using 36 MeV Oxygen ions. Standard *npn* and IMC SiGe HBT test structures were fabricated in a 130 nm, 200 GHz peak f_T SiGe BiCMOS process (IBM 8HP). Using these structures, a heavy-ion microbeam was rastered across a two-dimensional area covering the transistors, and terminal transients were captured on a high-speed oscilloscope. A setup identical to that reported in [54] was used.

For the standard *npn* SiGe HBT, the collector was biased to 2.0 V, with all other terminals grounded. A similar bias scheme was used for the IMC SiGe HBT, with the collector and upper base (B2) biased to 2.0 V, with all other terminals grounded. Fig.

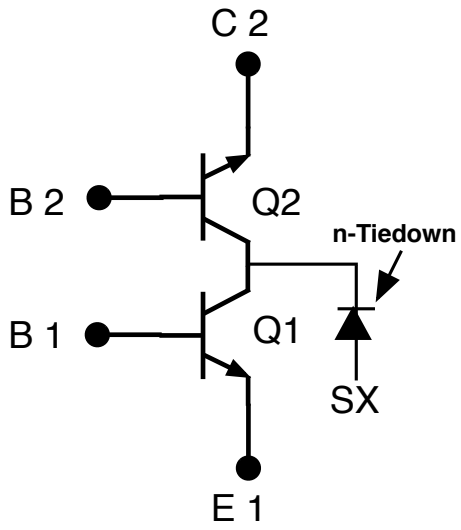


Figure 97: Schematic of IMC device with n-Tiedown connected to shared sub-collector.

98 shows the results of the TRIBICC experiment, highlighting the over 75% decrease in the peak current transient over a standard bulk SiGe HBT. Additionally, the IMC device shows approximately a 50% reduction in the magnitude of the diffusion tail between 0.5 - 1.5 ns.

The peak collector current transients are greatly reduced in the IMC device, as shown in Fig. 99, which presents a direct comparison of 2-D transient sensitivity between the standard SiGe HBT and the IMC SiGe HBT with n-Tiedown. This reduction in ion-induced current transients is attributed to both the IMC device topology and the use of the n-Tiedown to shunt away deposited carriers in the sub-collector. By integrating the collector current of a single transient at each strike location, the total collected charge across the device is shown in Fig. 100, further highlighting the ability of the IMC device to mitigate the charge deposition at sensitive nodes from an ion strike. Therefore, the IMC approach represents a simple technique to reduce both (fast) peak current transients and (slow) diffusion current transients associated with ion strikes, with obvious SEU mitigation benefits.

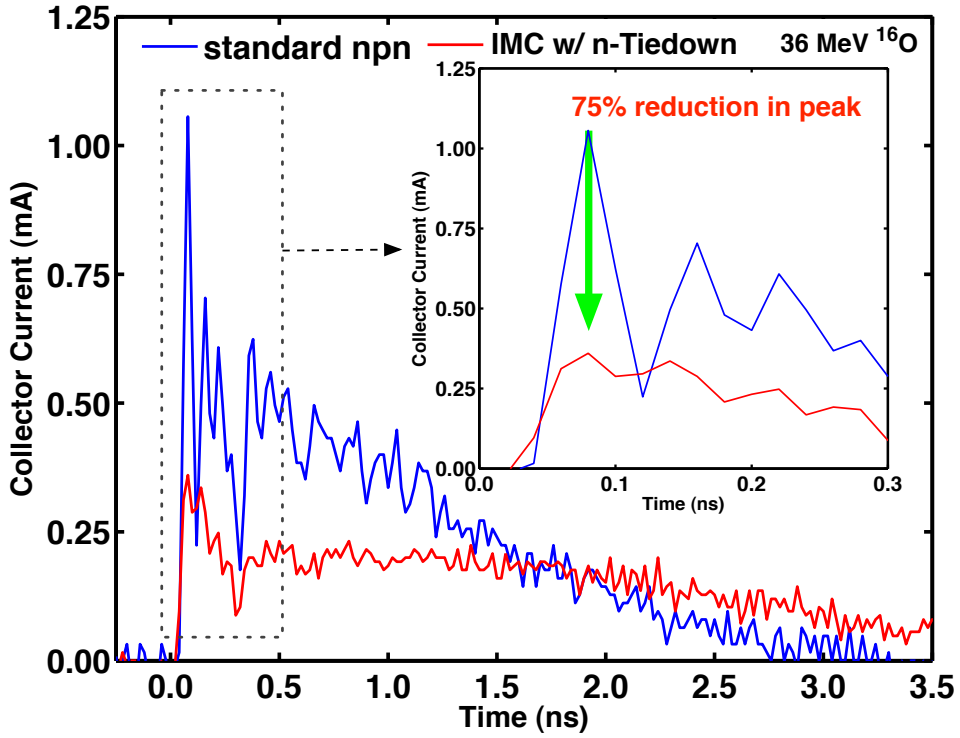


Figure 98: TRIBICC (36 MeV ^{16}O) results of worst case collector current transient, highlighting improvement of IMC SiGe HBT with n-Tiedown. Inset highlights the decrease in peak current transient.

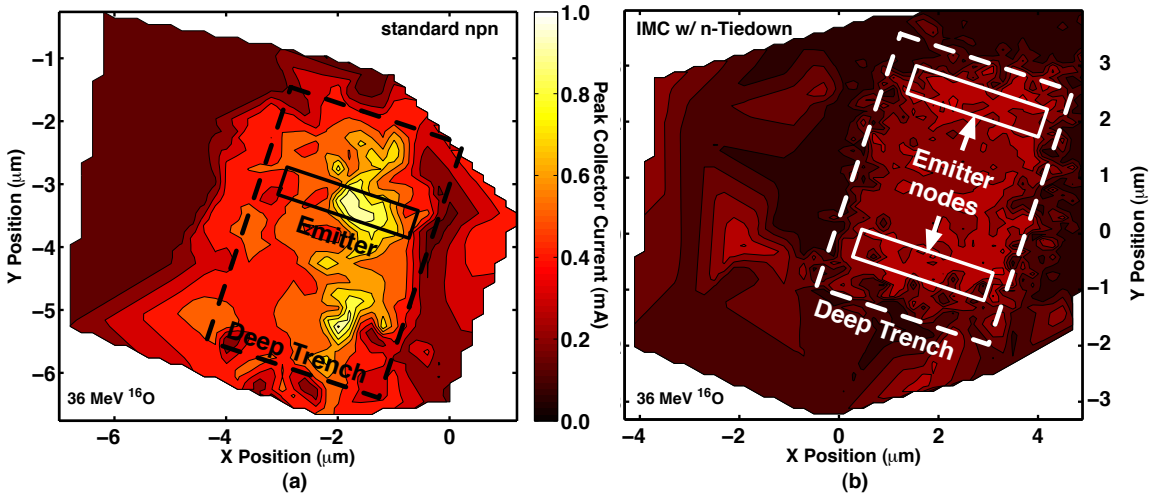


Figure 99: 2-D color-map of peak collector current transient from ion microprobing (36 MeV ^{16}O) of both standard *npn* (a) and IMC with n-Tiedown (b). The deep trench ring and emitter nodes represent the approximate location of the HBT.

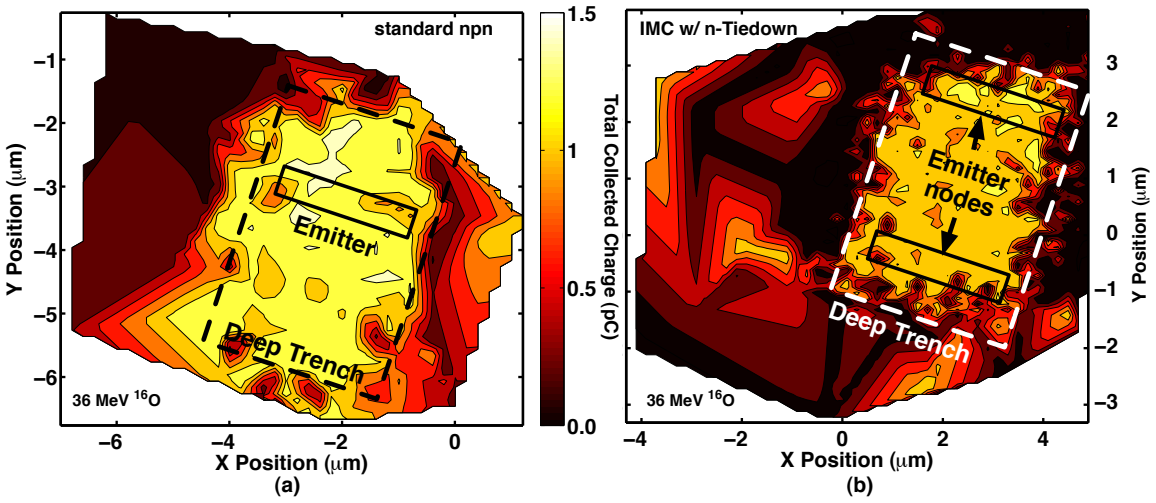


Figure 100: Ion microprobing (36 MeV ^{16}O) results of total collected charge as integrated from position-based current transients for both standard *npn* (a) and IMC with n-Tiedown (b), highlighting the decrease in collected charge of the IMC device.

5.2.3 IMC Shift Register Design

In order to implement the IMC device in digital circuit blocks, slight modifications are necessary in order to accommodate the cascode topology. The digital circuit designed was a 16-bit SR containing a D-flip flop (DFF) in a master-slave configuration. A SR was chosen since it allows straightforward experimental verification of the SEU response [30].

The main modification in the IMC SR design was in the storage cells in the DFF. The most sensitive nodes of a standard DFF are the devices X1 – X6, as shown in Fig. 101, which were replaced by IMC devices. Q1 and Q2 serve as level-shifters, allowing the addition of the inverse cascoded device in the storage cell. The B2 node of the IMC device requires a fixed *dc* potential to prevent the bottom device (Q1) from entering saturation. Therefore, the IMC devices used in the clock gates (X5 – X6) the top device (Q2 from Fig. 97) is diode connected, while in the differential cells (X1– X4), Q2 from Fig. 97 is connected to ground (highest potential). The DFF operates from a VEE of -5.2 V, which is sufficiently high enough to accommodate the additional VBE drop required by the IMC topology. For this IMC design, since the

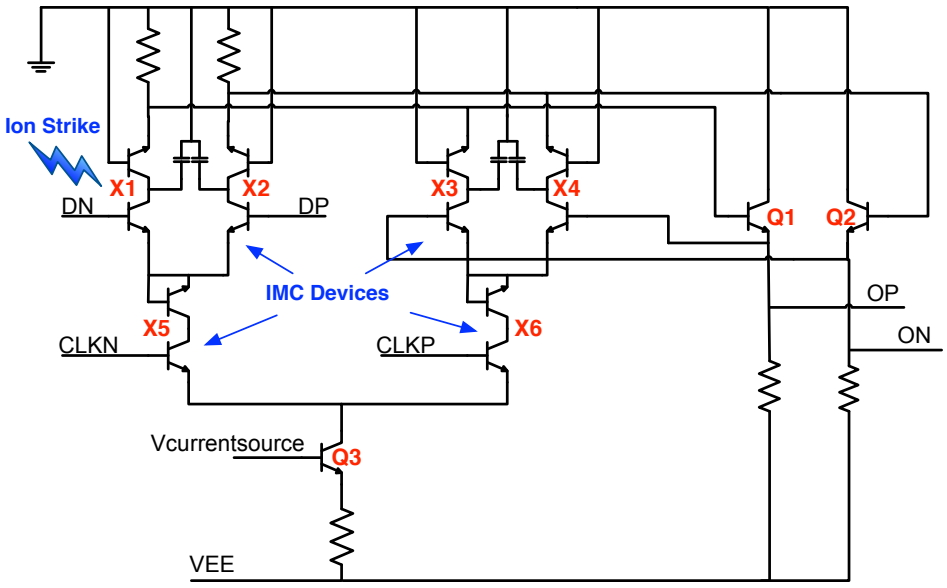


Figure 101: D flip-flop with IMC devices inserted in critical nodes. Q1 and Q2 level shift the signal to accommodate the cascode topology.

n-Tiedown is not modeled in the design kit, a small capacitor (100 fF) was connected to the C-tap node to shunt away excess charge generated during an ion strike.

To theoretically verify the benefits of the IMC device in the SR, a current transient from a calibrated 3-D model [63] was injected into the shared sub-collector node of a single device in the DFF using the Spectre simulation tool within the Cadence design environment. Fig. 102 shows the data and output signals from the DFF, both with and without a C-tap capacitor. The results without the capacitor clearly show a bit error due to the ion strike at 5.6 ns. However, for the device with a 100 fF capacitor connected to the sub-collector node, no error occurs (although there is a slight distortion in the waveform). If a slightly larger capacitor is used, the distortion can be minimized at the expense of reduced circuit speed.

To verify SEU peformance using the IMC approach, 16 bit SRs were designed in a first-generation 0.50 μm, 50 GHz peak f_T SiGe BiCMOS process (IBM 5AM). The SR variants we designed included a standard *npn* SR and an IMC SR with a 100 fF capacitor connected to the sub-collector node of the IMC SiGe HBT. Due to

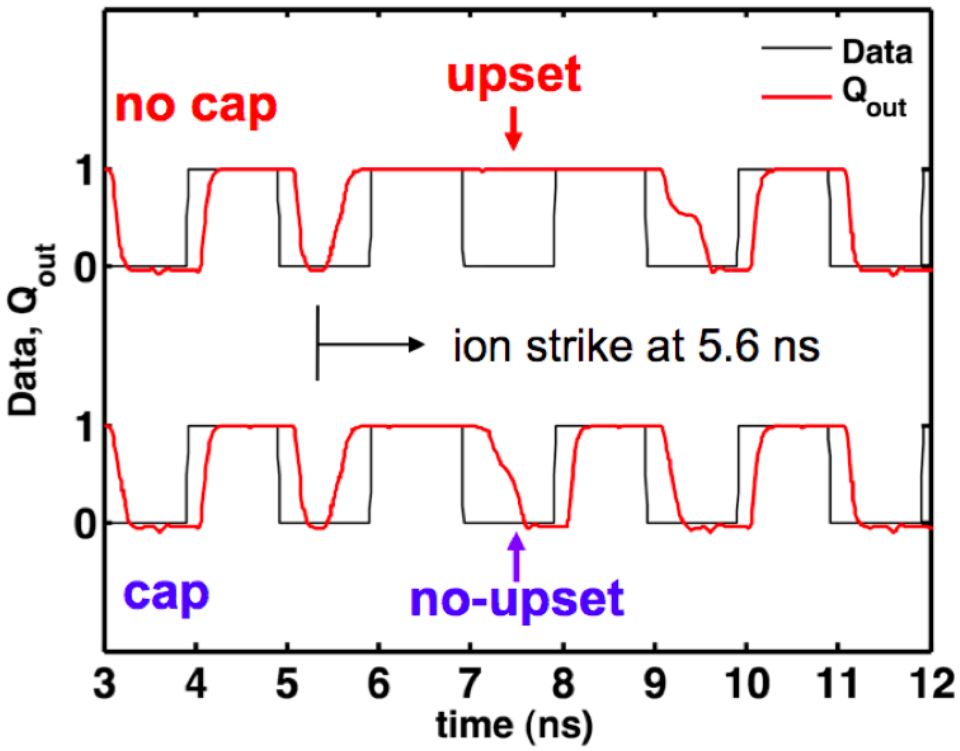


Figure 102: Spectre simulations of an ion strike in a DFF using IMC device both with and without capacitor.

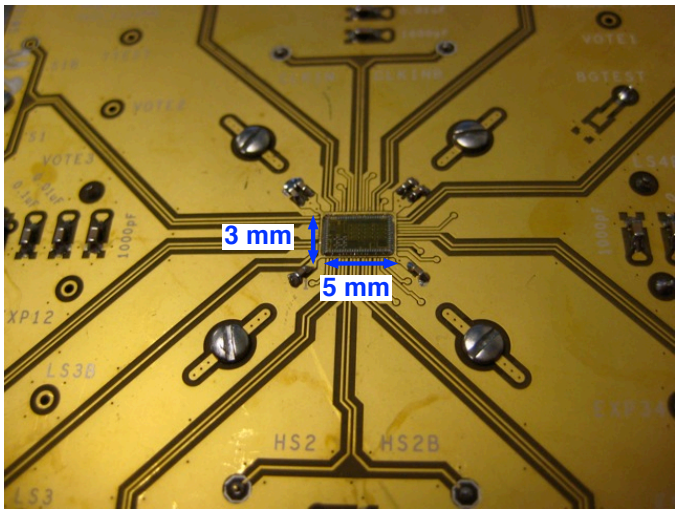


Figure 103: Picture of packaged IMC shift registers.

the groundrules of this SiGe technology, the IMC SiGe HBT is 2x larger (DT area) than the *npn* SiGe HBT (a single C-B-E device); however, the total IMC SR size is negligibly larger than the standard SR. The SRs were packaged in a high-speed fixture featuring low-loss microstrip feed lines and SMA I/O for maximum bandwidth. A picture of the shift registers mounted in the package is shown in Fig. 103. Each 3x5 mm^2 die contains 3 shift registers sharing the clock and input data to reduce the number of high-speed I/O necessary on the package. All SRs operated from a -5.2 V supply and each DFF consumed 1.0 mA of tail current. The performance for the standard *npn* SR was clocked to a maximum error free operation of 2.5 Gb/s, and the IMC SR achieved maximum speed of 1.0 Gb/s. The decrease in IMC performance is expected, and is largely due to the lower IMC device performance together with the small capacitor added at the C-tap node; however, the IMC SR still maintains adequate performance for Gb/s speed and can be further optimized depending on the speed required.

5.2.4 Heavy-Ion Broad-Beam Shift Register Characterization

In order to verify that the reduction in transient currents and collected charge translates into increased radiation hardness, heavy-ion broad-beam characterization was

performed at the Texas A&M Cyclotron Institute. Using an Anritsu bit error rate tester (BERT), 16-bit standard master/slave (*npn* only), standard cascode, and IMC SRs were compared under irradiation from various ion species. All of the SRs had a similar topology and clock distribution, thus making direct comparisons possible. The circuits were exposed to 15 MeV/amu Neon, Argon, Xenon, and Krypton, and 25 MeV/amu Nitrogen to provide sufficient range of linear energy transfer (LET) rates from 0.885 to 56.2 MeV cm^2/mg. The SRs were measured with a 500 MHz clock and irradiated to achieve 100 errors or more when possible with the final error count (includes single and multiple bit errors) and fluence recorded. The clock and data signals were fed into the high-speed package through SMA cables and connected directly to the BERT.

From the measured fluence and the total number of errors, an error cross section (σ) can be determined, which is a measure of the amount of sensitive area in the circuit for a given LET. Graphing error cross section vs. LET provides a metric to gauge the effectiveness of radiation hardening techniques [29]. The two main components of this curve are the saturated cross section and the threshold LET. The saturated cross section is the error cross section limit as the LET is increased, which should be minimized to improve radiation tolerance. The threshold LET is the minimum LET at which errors appear, and effective mitigation should raise this threshold. Fig. 104 plots the cross section versus LET for the standard *npn*, standard cascode, and IMC SR, with the dashed lines showing a Weibul fit to the measured data.

It is clear that for high LETs, the standard cascode and IMC SR behave similarly, but have a larger saturated cross section than the standard *npn* SR. This degradation is attributed to the increase in the deposited charge of higher LET species and thus, the capacitor tied to the C-tap node is not able to remove sufficient charge to prevent the error from occurring. In addition, a slightly larger DT area is required for the IMC device due to groundrule restrictions in the first-generation SiGe technology

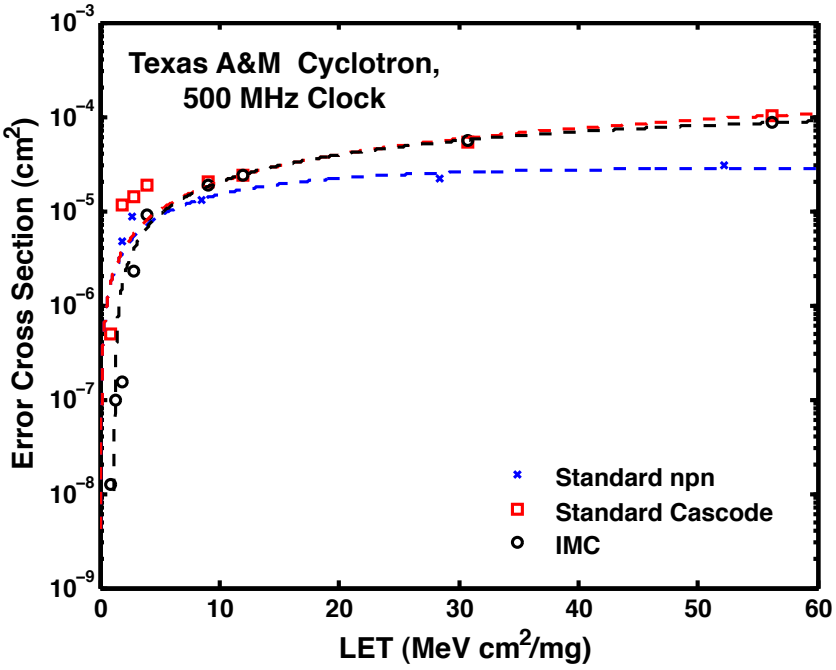


Figure 104: Heavy-ion broad-beam error cross section versus LET for standard *npn*, cascoded *npn*, and IMC shift registers.

used to fabricate these SRs. This slightly larger area will not impact overall circuit dimensions, but does degrade the performance at the higher LETs, and thus yields a similar saturated cross section as the standard cascode. Third-generation SiGe IMC devices will allow for a more compact layout, thus a reduced sensitive area, which should have a saturated cross section closer to the standard *npn* only SR. In addition, the capacitor may be replaced with an n-Tiedown, which may be able remove more charge.

Even though at high LETs the IMC is softer than the standard *npn*, at lower LETs, the capacitor is able to remove enough deposited charge to prevent bit upsets from occurring. The improved radiation response can be clearly seen in Fig. 105, which shows the standard *npn* and IMC SRs from LETs ranging from 0 - 10 MeV cm^2/mg. Clearly, the threshold LET is increased, from approximately 0.1 MeV cm^2/mg for the standard *npn* to over 1.2 MeV cm^2/mg for the IMC SR, with over a 75% reduction in errors at LETs below 1.5 MeV cm^2/mg.

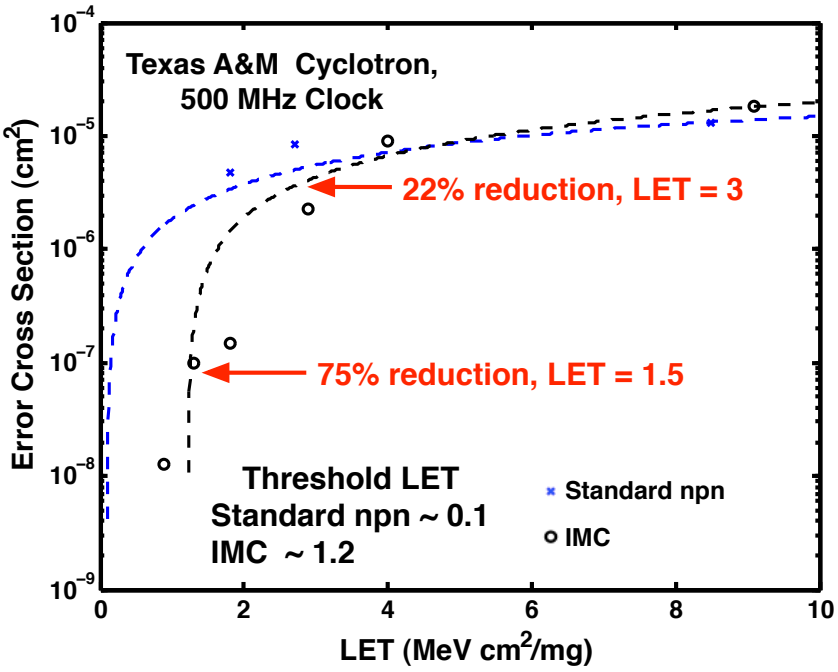


Figure 105: Zoomed error cross section versus LET for standard *npn* and IMC shift registers, highlighting the SEU hardening from the IMC devices at low LETs.

To understand the potential system-level benefits of the reduced cross section at low LETs, the CREME96 tool [85] for SEE rate prediction was used to determine the reduction in errors for a typical satellite mission. This tool allows an orbital scenario to be configured and error rates are determined given a predicted distribution of particles. The simulation was configured for a geosynchronous orbit, with 100 mil of aluminum shielding and a solar minimum, maximum, and worst day particle spectrum, as shown in Fig. 106. The Weibul fit parameters from the measured broad-beam data were entered into the simulation tool, with the sensitive volume estimated based on error count and total device size. The IMC device was estimated to have a larger sensitive volume due to the slightly larger device size and therefore these results represent a worst case scenario.

Comparing the σ-LET (Fig. 105) and particle flux-LET curves (Fig. 106), it is clear that almost all of the particles have an LET of less than unity. Since the IMC SR has a threshold LET of 1.2, most of these particles will not cause an upset and will

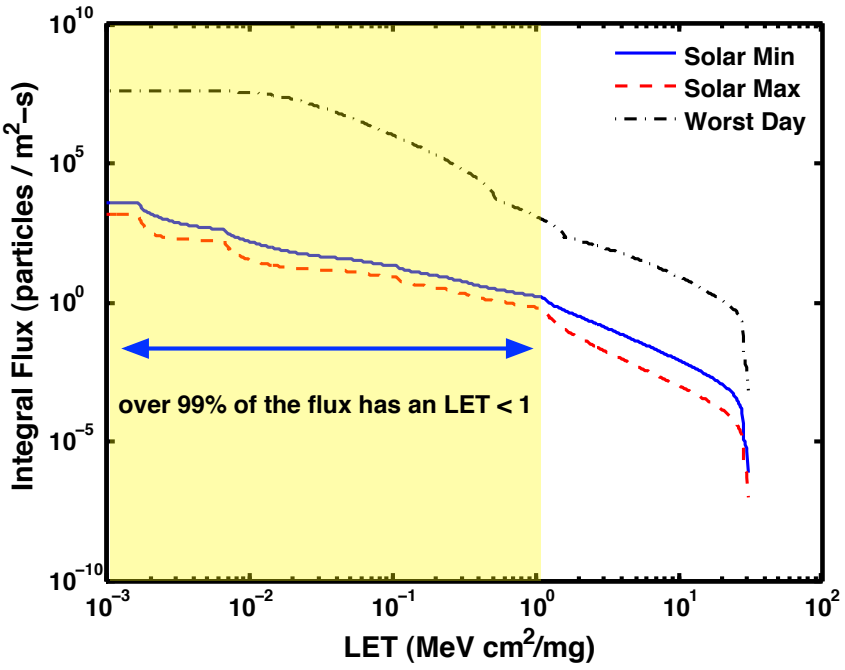


Figure 106: LET Spectrum of Geosynchronous orbit through 100 mil of Al from CREME 96. Highlighted region shows over 99% of flux is below an LET of unity.

Table 8: CREME 96 orbit simulation results of shift registers

	Errors / bit / day[1]		Reduction in Errors
	STD *npn*	IMC	
Solar Min	3.24E-04	1.05E-04	68%
Solar Max	1.19E-04	3.88E-05	67%
Worst Day	3.23E+01	4.77E-01	99%

[1] with 100 mil of Al shielding

result in an increased SEU tolerance even with a larger saturated cross section. Table 8 highlights the reduction in errors for three orbital scenarios of the IMC SR over the standard *npn* SR. For solar minimum and maximum models, the IMC device exhibits almost a 70% reduction in bit errors per day, with the worst day model showing an almost 100% reduction.

5.2.5 Summary

We present ion microprobing results confirming the potential benefits of using the IMC SiGe HBT for low-overhead SEU mitigation, discuss the design tradeoffs of a high-speed SR implemented using this new RHBD approach, and demonstrate the mitigation benefits using a heavy-ion beam. The ion microprobing results of a third-generation IMC SiGe HBT with n-Tiedown demonstrated a large reduction in transient response from an ion strike, which should help reduce SEU sensitivity with no overhead.

In addition, we present the first functional IMC circuit using a first-generation IMC SiGe HBT in a modified SR topology, with little area or power penalty over a standard *npn* SiGe HBT SR, achieving 1.0 Gb/s operation. To verify the radiation hardening benefits of the IMC device, the SRs were measured under a heavy-ion beam to determine the error cross section of these RHBD circuits. The results show that the threshold LET is increased for the IMC SR, with greater than 75% reduction in error cross section at LETs below 1.5 MeV cm^2/mg. Using the CREME 96 simulation tool, the potential on-orbit benefits of the IMC device were shown to translate into approximately a 70% decrease in bit errors per day for a GEO orbit.

These measured results present a compelling case for investigating the use of IMC devices for use in high-speed space based digital circuits. The IMC device does not require extra processing steps, power, or significantly larger area. This simple design modification can enable increased radiation tolerant circuits, using low-cost and high-speed commercially available SiGe technology. Using these devices in digital control components for active T/R modules could provide SEU mitigation that would prevent errors from occurring and allow the antenna system to operate reliably in radiation environments.

CHAPTER VI

CONCLUSION

6.1 Summary of Contributions

The purpose of this research is to provide insight into the design and performance of high-frequency SiGe BiCMOS circuits for use in extreme environments. Developing components using a commercially available SiGe technology that are able to withstand extreme environments is very advantageous due the technologies low-cost and high-performance, with the ability to create next-generation space-based wireless systems. Specifically, these designs were targeted towards components used in integrated active phased-array antenna systems, like those for radar and wireless communication. The feasibility of fabricating an antenna system using SiGe circuit blocks was demonstrated. In addition, RF performance metrics over a wide-temperature range were characterized, which required development of novel measurement setups. Lastly, radiation effects on RF and digital building blocks used in integrated T/R modules were examined and SEE mitigation techniques are presented and verified. The specific contributions include:

1. Design and characterization of an ultra-low power SiGe HBT X-band LNA for use in high-altitude radar and wireless communication systems. The LNA achieves less than 2 dB noise figure and 10 dB gain while only dissipating 2 mW.

2. Design of a high dynamic range SiGe HBT X-band LNA that achieves over 30 dB of gain, 30 dBm OIP_3, and less than 2.5 dB noise figure.

3. Characterization of the robustness of three different LNAs under large-signal

RF stressing conditions to determine degradation of operating LNAs under such conditions.

4. Development of an integrated SiGe BiCMOS X-band T/R module, containing LNA, T/R switch, phase shifter, and PA. The T/R module was designed using a third generation SiGe BiCMOS technology and included RF, analog, and digital blocks. This T/R module is to serve as the RF front-end for an active phased-array antenna system.

5. Integration and assembly of 64 element active phased array receive antenna using integrated SiGe T/R modules on a multi-layer organic packaging substrate. 8 SiGe T/R modules were integrated directly onto the organic, slot-fed, aperture coupled microstrip patch antenna. The integrated assembly was characterized in a near field antenna range, and was measured to have over 25 dB of antenna gain.

6. Characterization of packaged SiGe HBT X-band LNAs under deep-cryogenic operating conditions. These LNAs were measured to have noise figures of less than 21 K at X-band.

7. Design of novel on-wafer wide-temperature high-frequency noise measurement setup. This setup allows accurate noise figure measurement across a wide temperature range by accurately calibrating input and output feed line losses and the use of a passive resistor test structure to correctly calibrate temperature effects. The in-line network analyzer allows for in-situ S-parameter measurement.

8. Characterization of low-temperature noise figure of SiGe HBT devices and a low power LNA. The SiGe HBT device was characterized from 296 to 150 K, over a range of collector currents, with a minimum noise figure of 0.5 dB at 150 K. In addition, a low-power LNA was characterized from 300 to 193 K whose

noise figure decreased from 2 dB at room temperature, to approximately 1 dB at 193 K.

9. Design of on-wafer wide-temperature two-tone linearity measurement setup using a network analyzer and signal generator. The measurement setup allows for both swept power or swept frequency.

10. Measurement of two-tone linearity of a low power LNA from 300 to 173 K. The input and output TOI improved from 300 to 218 K, but was slightly degraded from 218 to 173 K. The reason for this degradation could be due to changes to the effective bias region as the devices are cooled. Therefore, for LNAs requiring high linearity across wide-temperature ranges, adjustments to the bias circuitry are necessary.

11. Investigation of total dose radiation effects on SiGe BiCMOS and CMOS only phase shifters. Both circuits were radiated to multi-Mrad, with no noticeable RF performance degradation. The BiCMOS phase shifter exhibited changes to the bias currents, potentially due to increased leakage in the nMOS bias current mirrors. The CMOS phase shifter currents experienced the largest percentage change in bias currents due degradation of the nMOS digital inverters, which would not effect RF performance.

12. Design of a novel SiGe HBT based device for use in radiation tolerant digital circuits. The device, called the inverse-mode cascode (IMC), is a composition of a cascode circuit topology with the upper, common base device operating in the inverse mode. The IMC device provides isolation between the sub-collector and the circuit output, which can be exploited to reduce single-event effects (SEE). An IMC SR was measured to have an increase in the threshold LET, as well as simulated results show a possible 70% reduction in errors over a standard npn only SR when operating in a geosynchronous orbit.

6.2 Future Work

The research presented in this thesis are the initial results of investigating using SiGe BiCMOS technology high frequency circuits for phased-array antenna systems in extreme environments. Several opportunities for future research based on these results exist and can serve as follow on research for this work, and are summarized below.

A fully integrated receive only active antenna array was demonstrated. Future research can be conducted to fully implement a common transmit and receive antenna. The developed SiGe BiCMOS T/R chip contains the necessary hardware for transmit operation (T/R duplexer switch, PA, and bi-directional phase shifter). However, for a large integrated antenna panel, the PA design should provide robust to minimize chip-to-chip variation and simplified bias scheme. In addition, a T/R switch between the LNA and PA is necessary to switch between transmit and receive paths. In order to handle the higher output powers of the transmit side, as well as have low-loss to preserve receive SNR, a MEMS T/R switch is an optimal choice since it has a high compression point as well as low-loss.

Using the on-wafer wide-temperature noise figure and linearity measurement setups, additional devices and circuits can be characterized to better understand these RF characteristics over temperature. In addition to low-temperature measurement, high-temperature characterization can be conducted using these same setups and calibration techniques. Using these results, coupled with S-parameter measurements, higher order models of SiGe HBT devices can be created that would aid in development of RF circuits for wide-temperature operation. In addition, circuit designs with self-adjusting references can be developed, making use of the knowledge of how device and circuit performance change over temperature / bias, thus optimizing circuit performance for wide-temperature operation.

Radiation studies presented in this thesis demonstrate device and circuit block

level studies of components used in integrated high-frequency T/R modules. Testing fully integrated T/R modules in radiation environments (both for TID and SEE response) can aid in insight in designing radiation tolerant circuits. In addition, further investigation into using the IMC device for digital blocks, as well as developing standard radiation hardened logic cells using this device, could provide building blocks to implement the necessary digital logic for these modules.

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VITA

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